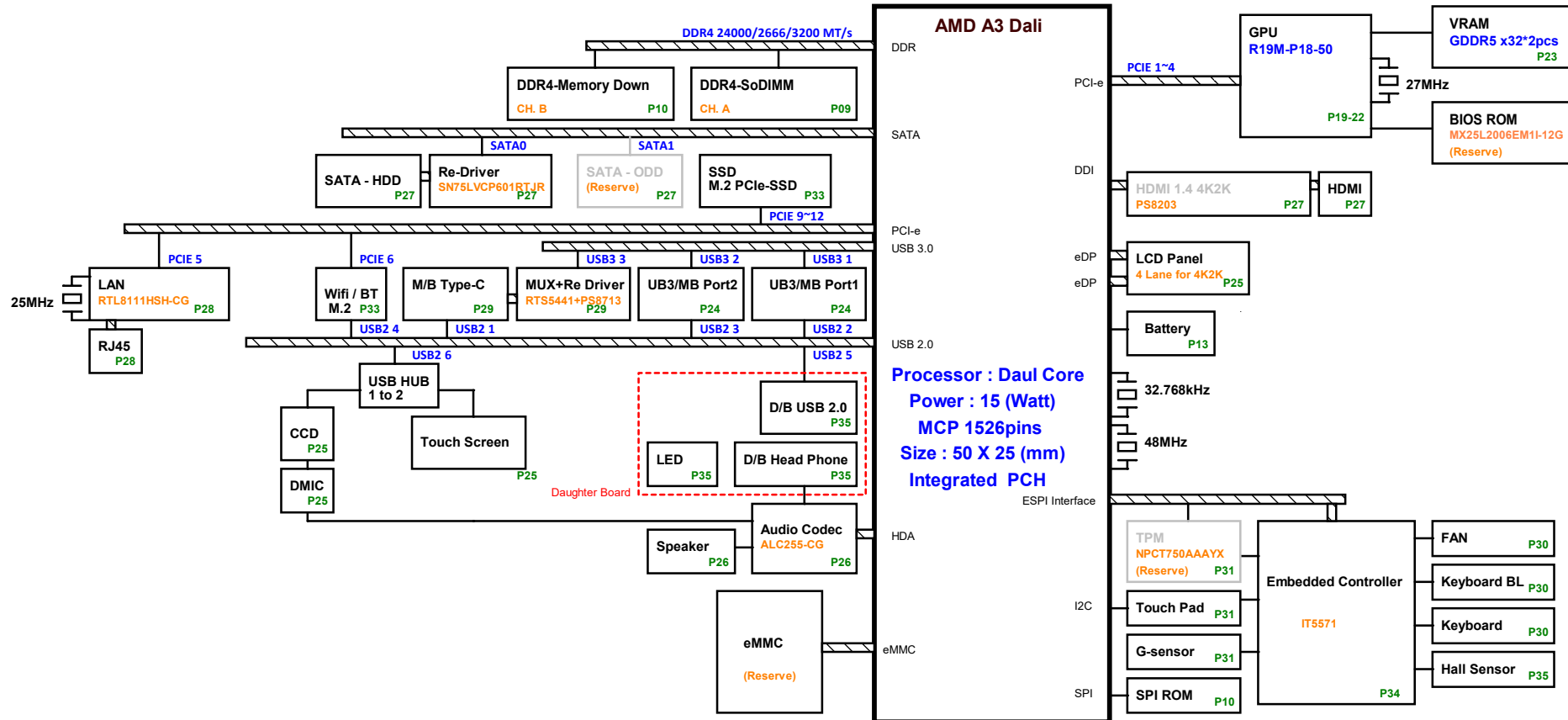
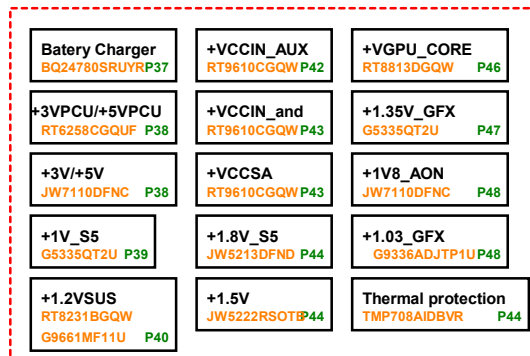


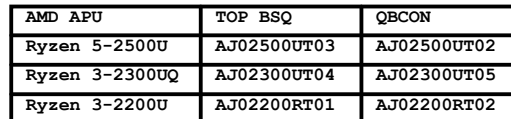
Z8E AMD A3 Platform Block Diagram

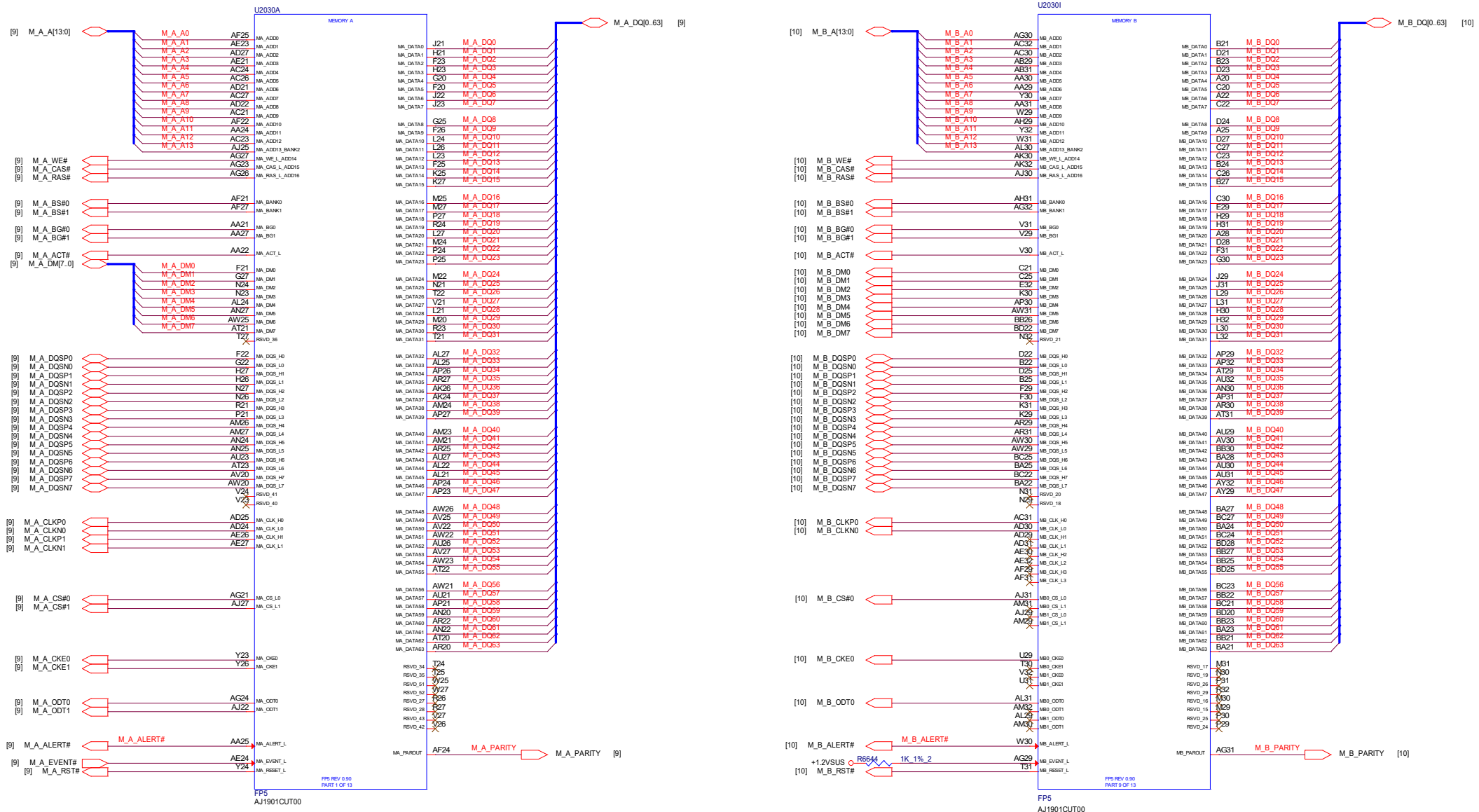
01

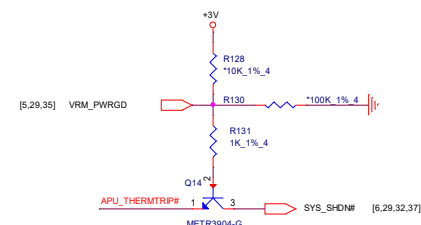


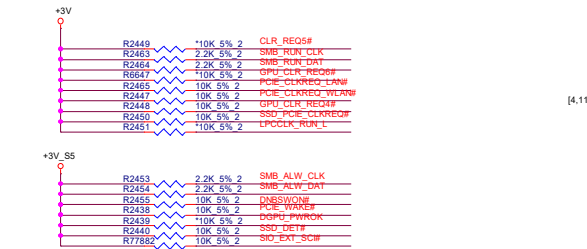
Power solution



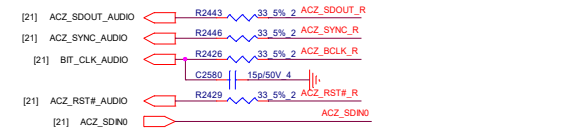




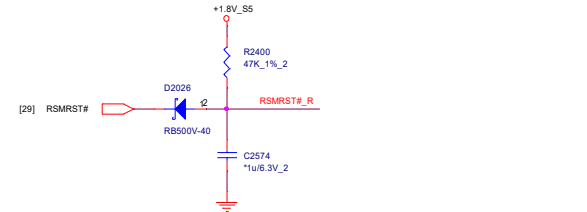




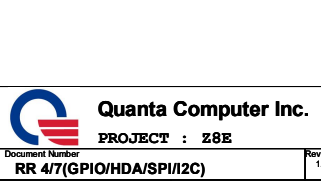
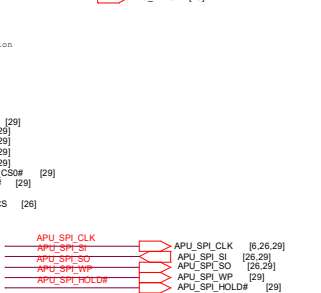
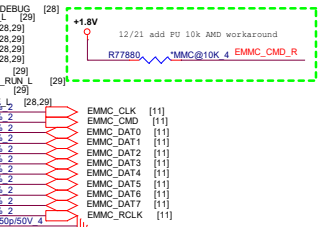
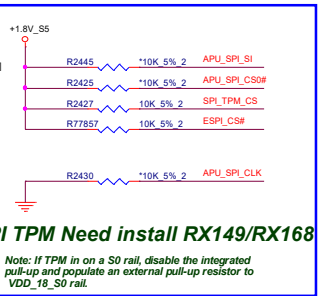
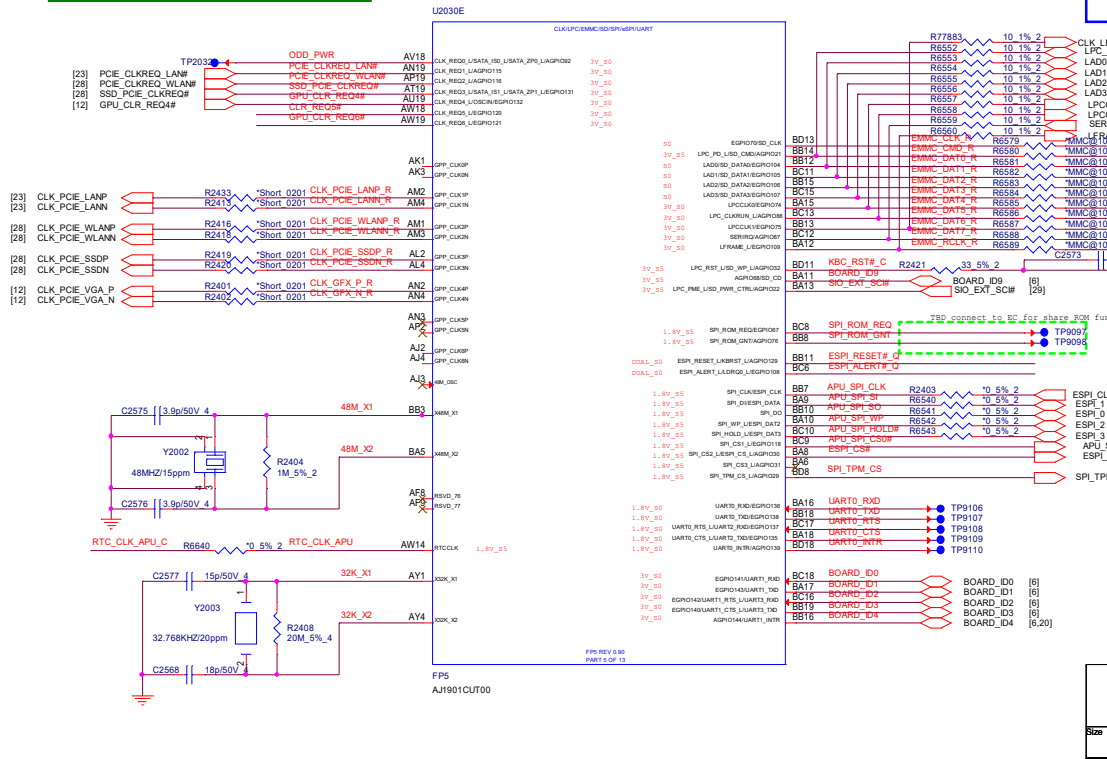
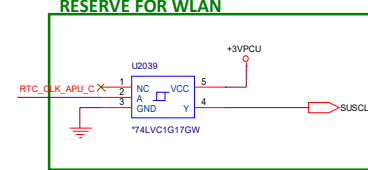
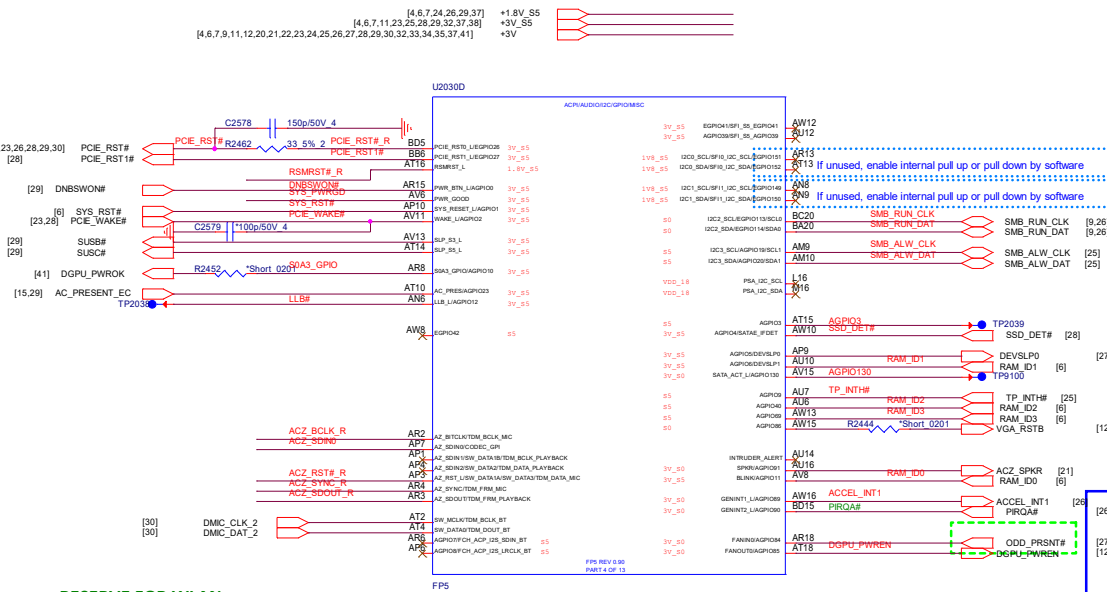
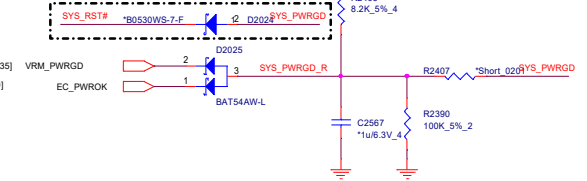
HDA INTERFACE



RSMRST_GATE# from EC

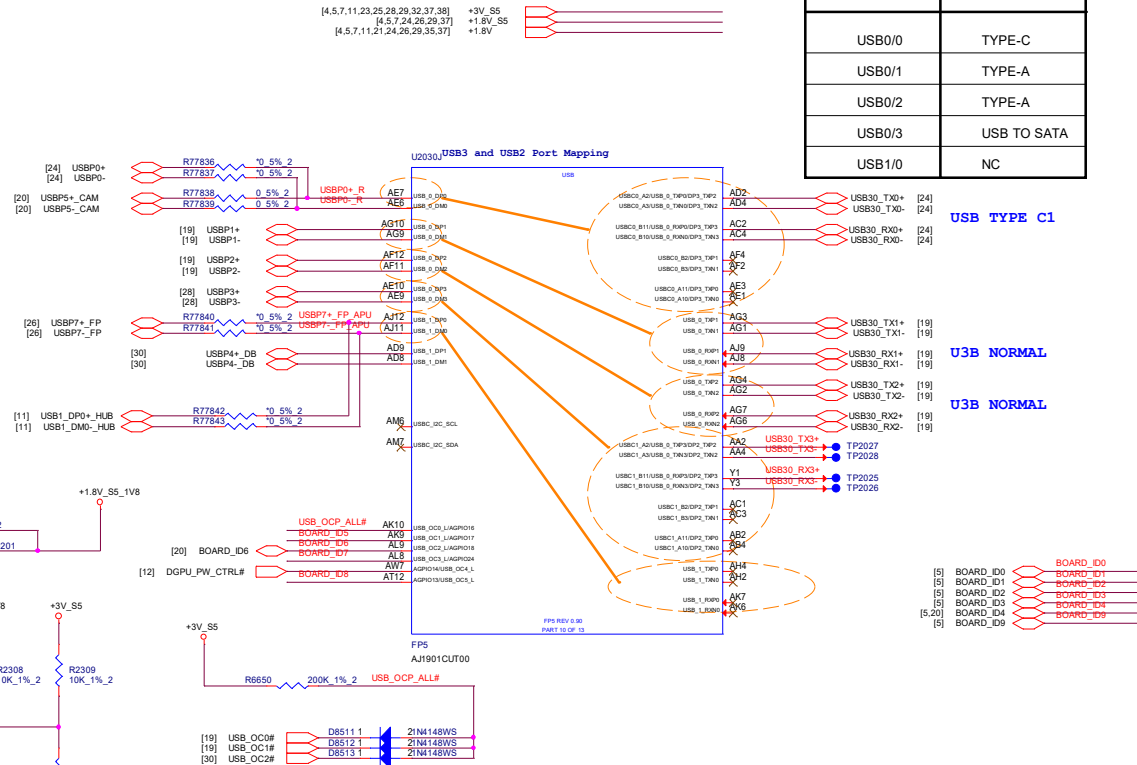


PWRGD CIRCUIT

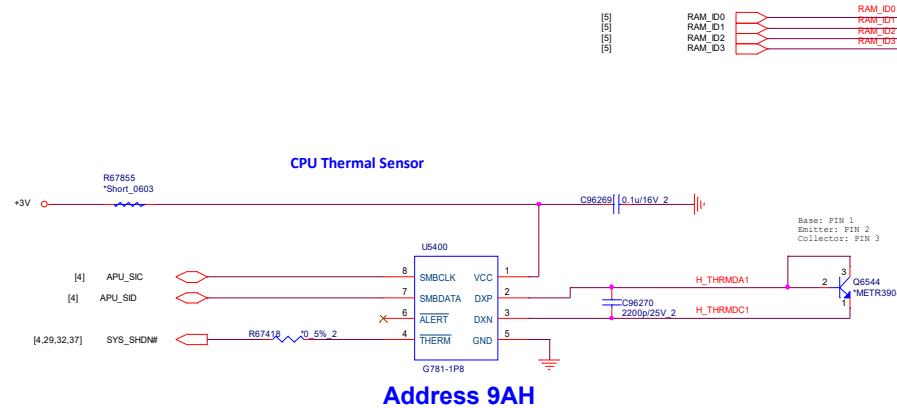


USB3 Port	Function
USB0/0	TYPE-C
USB0/1	TYPE-A
USB0/2	TYPE-A
USB0/3	USB TO SATA
USB1/0	NC

USB2 Port	Function
USB0/0	TYPE-C
USB0/1	TYPE-A
USB0/2	TYPE-A
USB0/3	BT
USB1/0	HUB
USB1/1	DB USB2



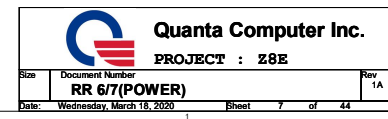
BOARD ID					
default	Low	High			
L	BOARD_ID0	Non eMMC	eMMC	S5	
H	BOARD_ID1	HDMI_N@	HDMI_R@	S5	
L	BOARD_ID2	Non G-sensor(GS_N@)	G-sensor(GS@)	S5	
L	BOARD_ID3	Non TPM(TPM_N@)	TPM(TPM@)	S5	
cable	BOARD_ID4	Non Touch panel	Touch panel-USB (Control by Cable)	S5	
H	BOARD_ID5	Non Type-C(TPC_N@)	Type-C(TPC@)	S0	
cable	BOARD_ID6	Single MIC(Cable control)	Dual MIC (DMIC@)	S0	
L	BOARD_ID7	GEN2	GEN3	S0	
L	BOARD_ID8	14"	15"	S0	
L	DGPU_PW_CTRL#	dGPU	UMA	S0	
L	BOARD_ID9	DALI	R3 PICASSO		

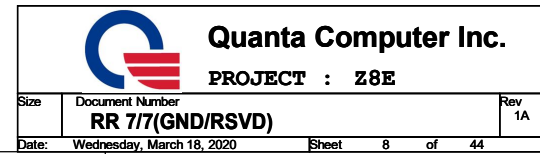


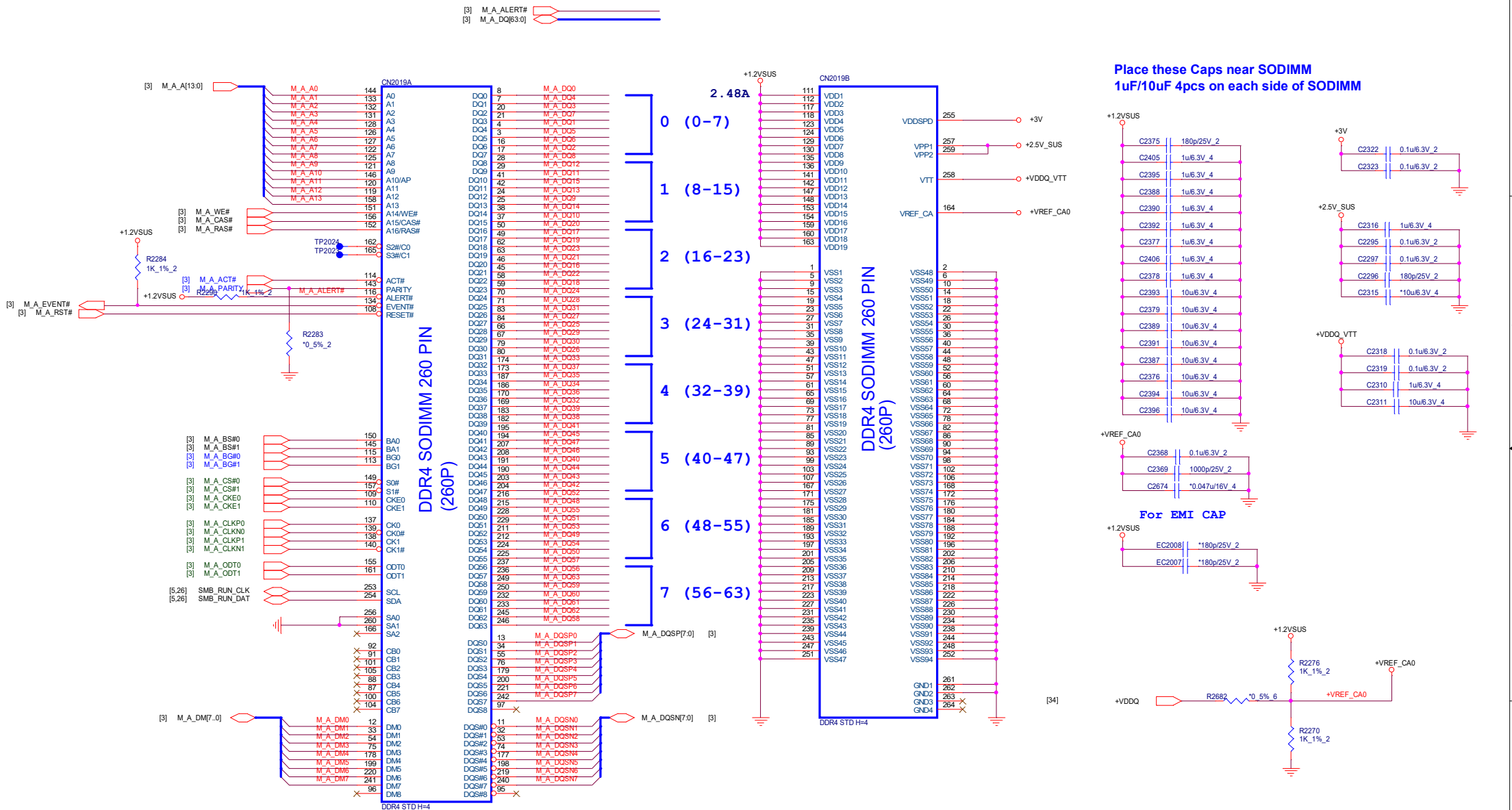
RAM ID

Schematic diagram for RAM ID. It shows a 3V_S5 supply connected to a network of resistors (R730, R385, R732, R378) and RAM chips (RAM_ID0, RAM_ID1, RAM_ID2, RAM_ID3). The resistors are labeled MD@10K, 5% 2. The RAM chips are labeled R783, R389, R737, and R389. The diagram shows the connection of the RAM_ID pins to the 3V_S5 supply through the resistors.

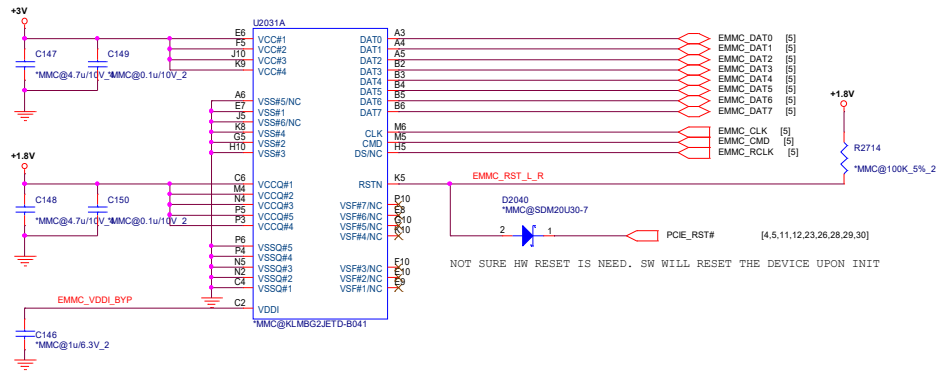
ID3	ID2	ID1	ID0	Vendor	Vendor PN	Quanta PN
0	0	0	0	Hynix 8Gb	HSAN8G6NCJR-VKC	AKD5QGSTW13
0	0	0	1	Micron 8Gb	MT40A512M16LY-075:E	AKD51ZSTL24
0	0	1	0	Micron 8Gb	MT40A512M16TB-062E:J	AKD5QGSTL23
0	0	1	1	Samsung 8Gb	K4A8G165WC-BCTD	AKD5QGST512
1	1	1	1	With out on board memory		



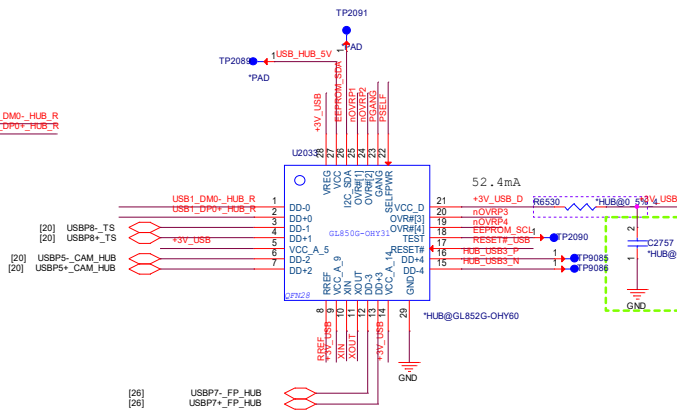
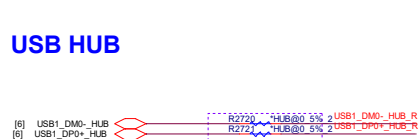




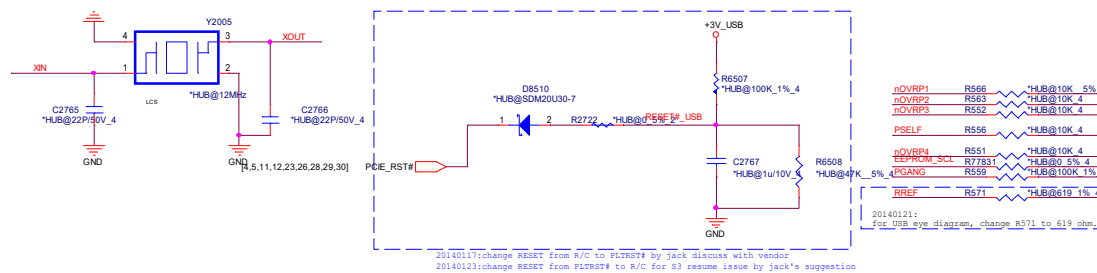
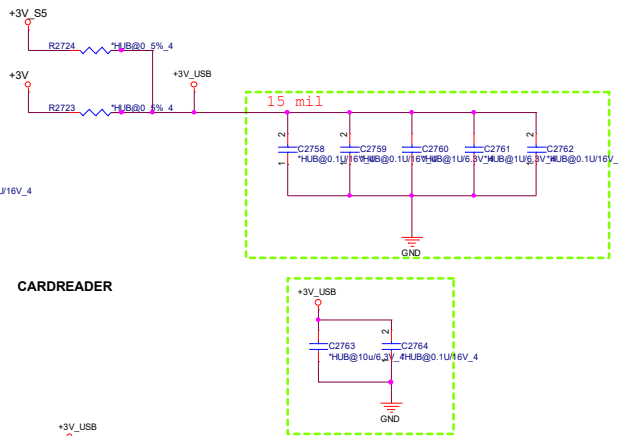


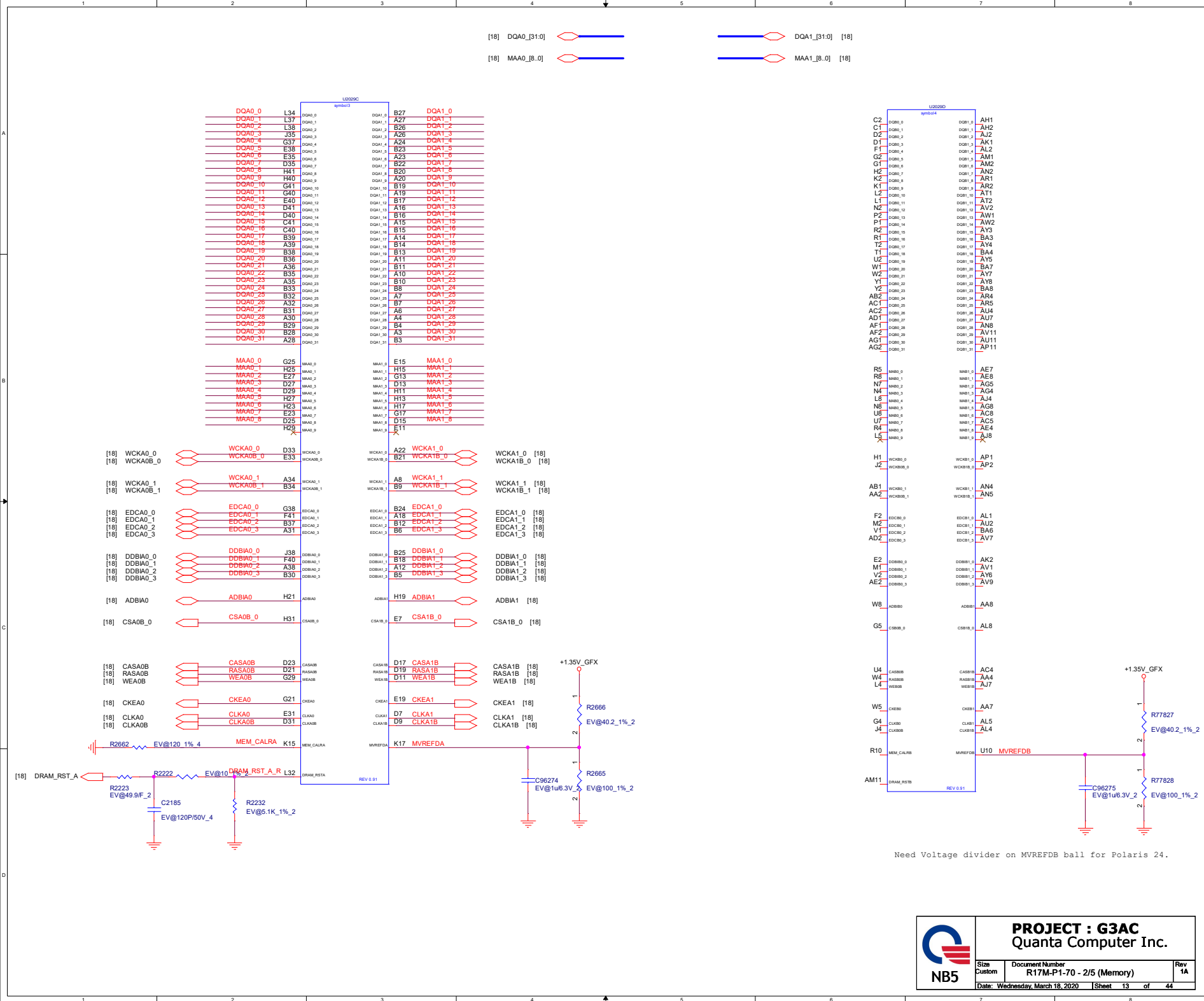


USB HUB

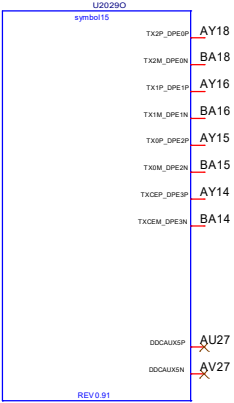


CARDREADER

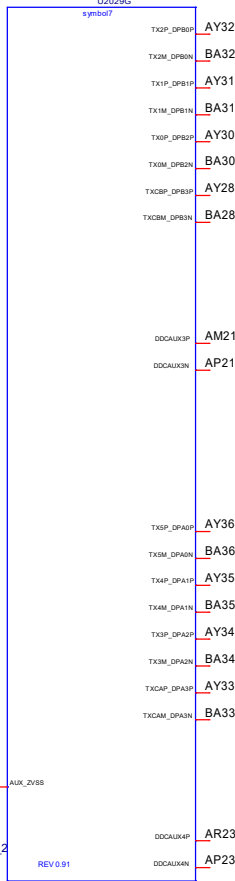




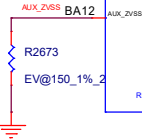
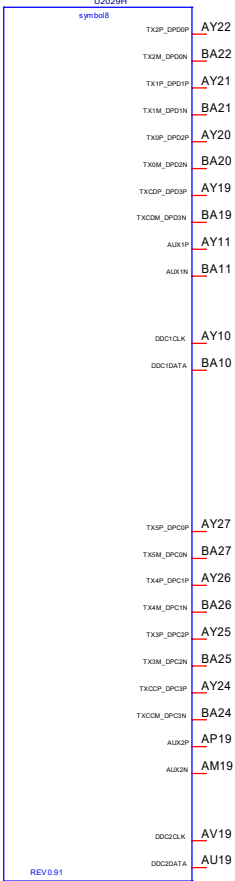
ASIC - TMDP (E)



ASIC - TMDP (A/B)

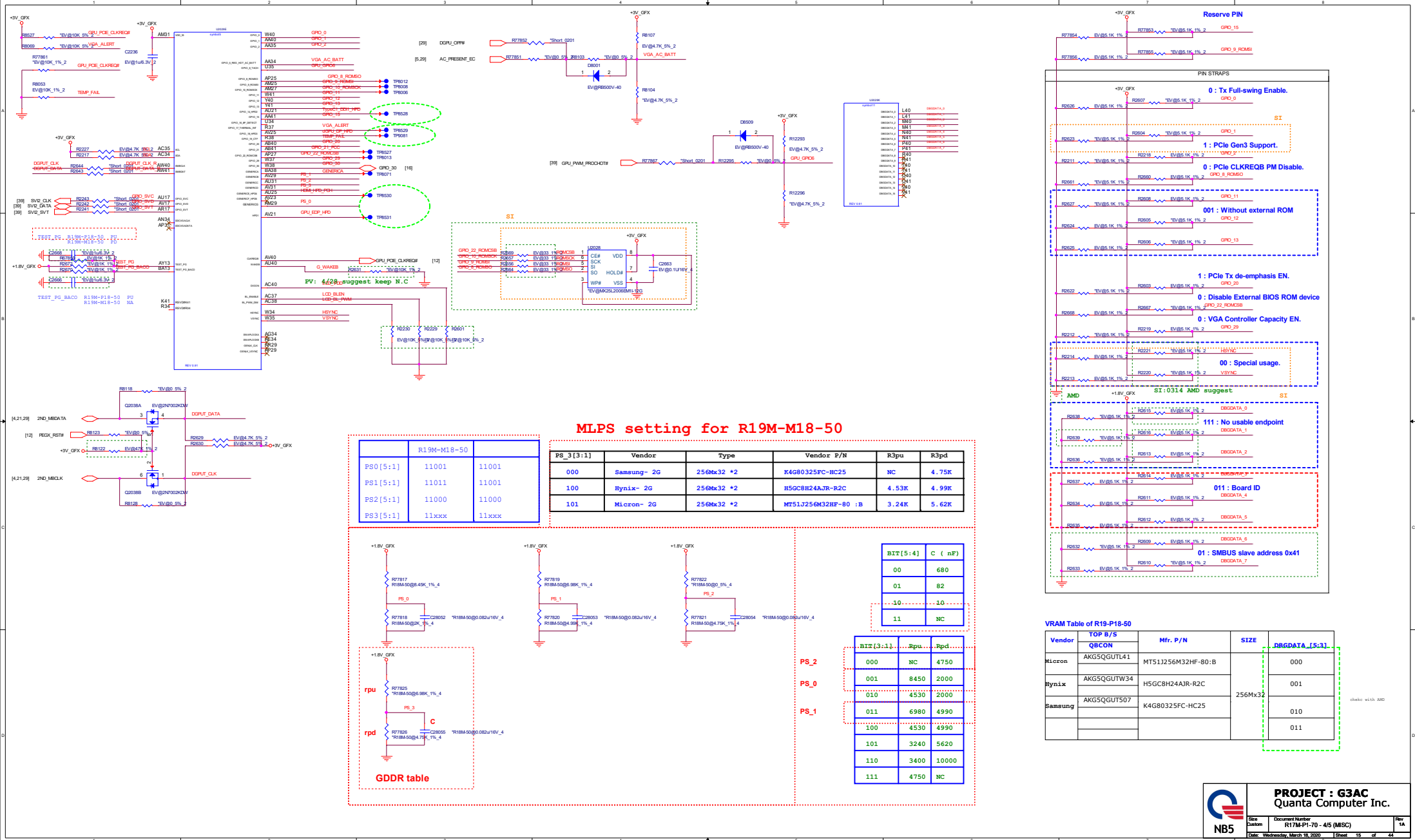


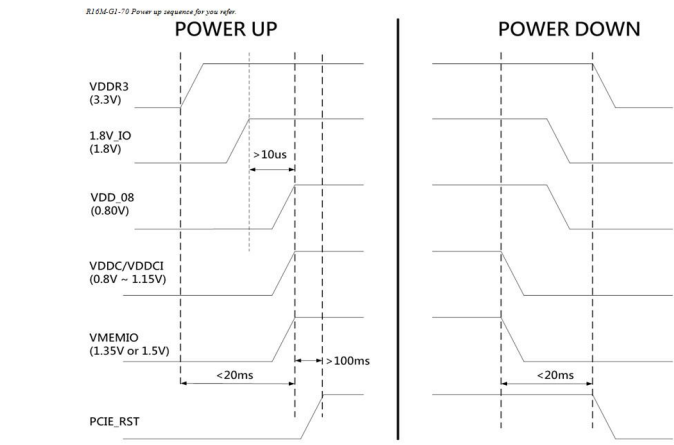
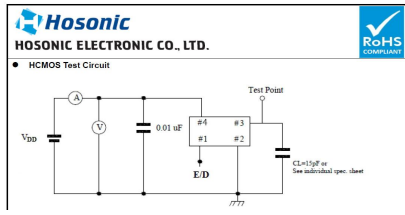
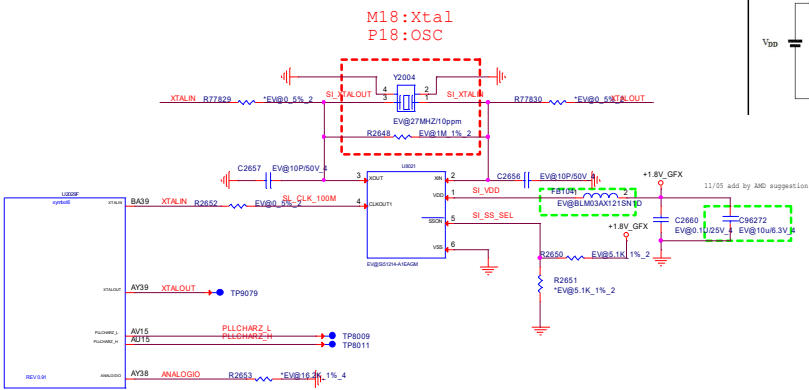
ASIC - TMDP (C/D)



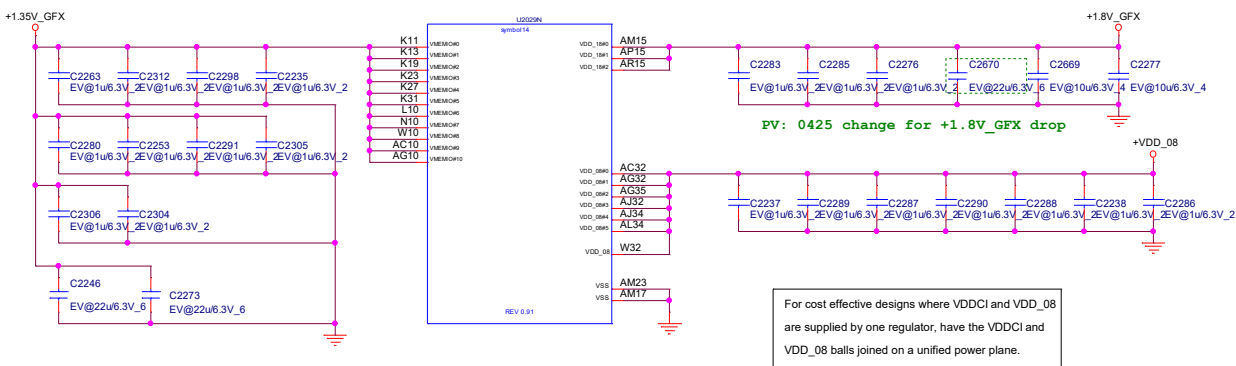
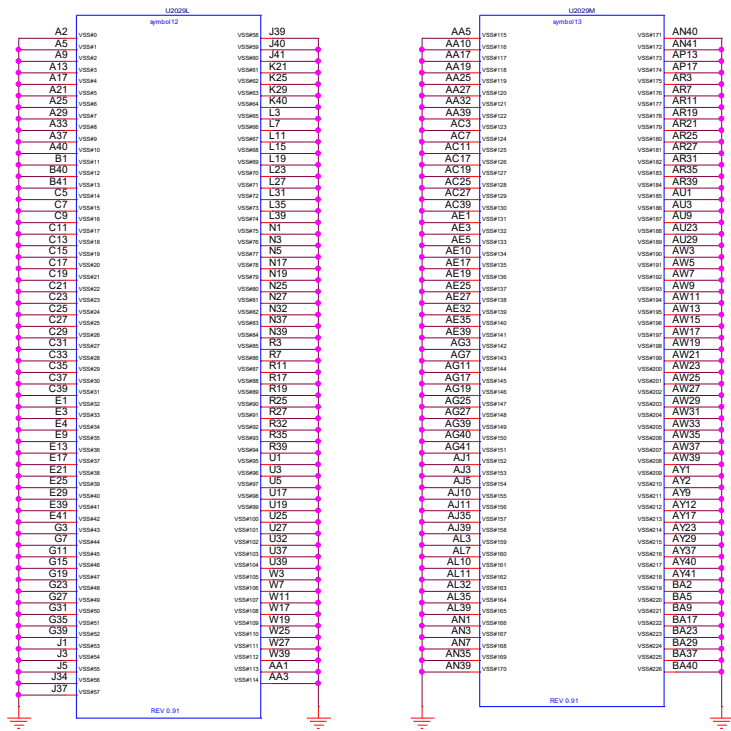
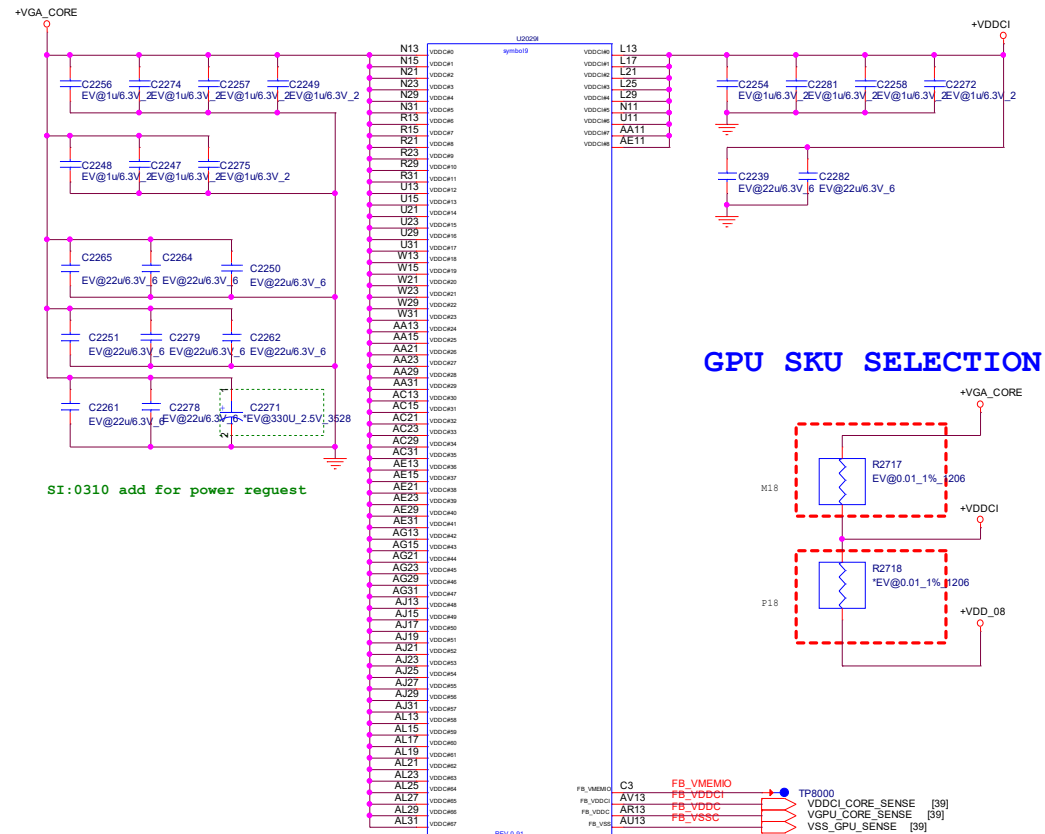
PROJECT : G3AC
Quanta Computer Inc.

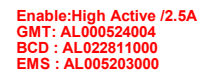
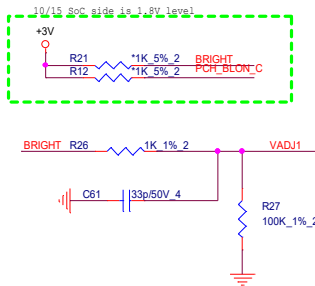
Size A3	Document Number R17M-P1-70- 3/5 (Display)	Rev 1A
Date: Wednesday, March 18, 2020		
Sheet 14 of 44		



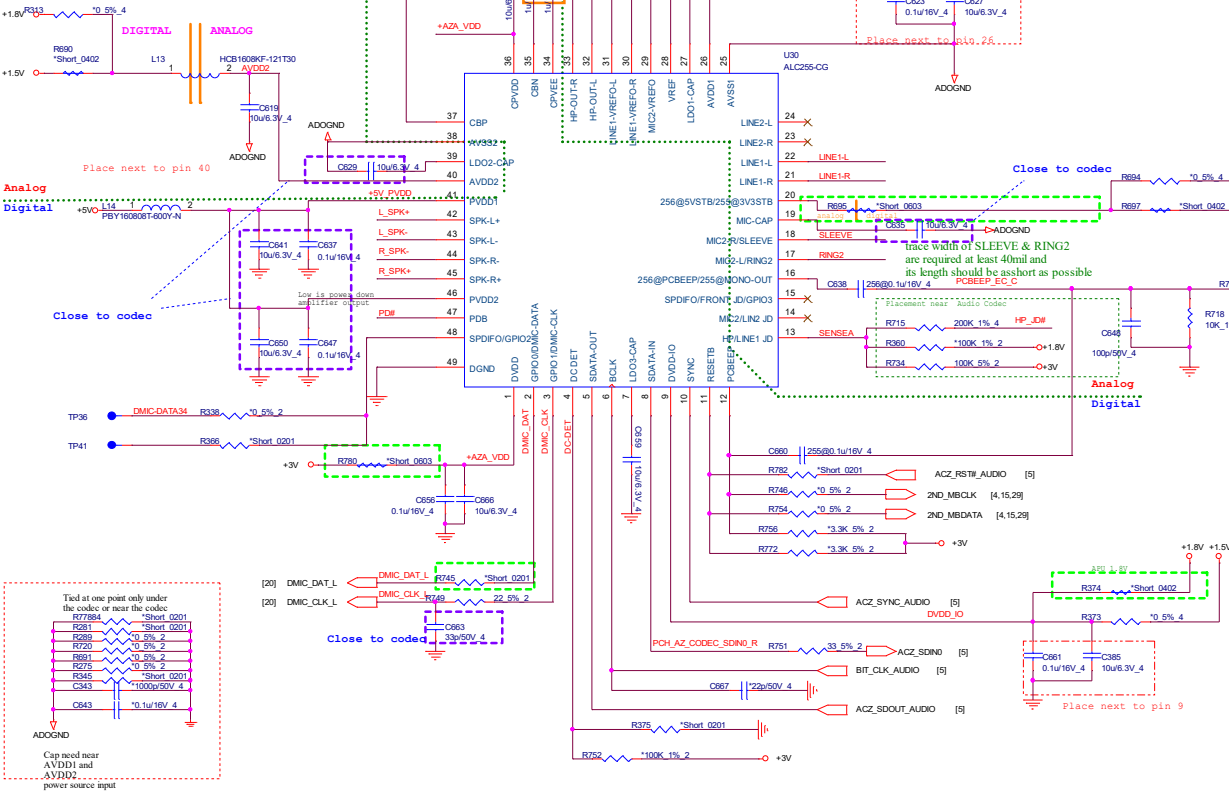


AMD GPIO Strapping	Setting	Name	Description
GPIO 29	Pull low 10K ohm	BIF_VGA_DIS	0: VGA Controller capacity enabled. 1: The device will not be recognized as the system's VGA controller (for headless designs).
GPIO 20	Pull up 10K ohm	TX_DEEMPH_EN	PCI Express transmitter deemphasis enable 0: Tx de-emphasis disabled. 1: Tx de-emphasis enabled.
GPIO 0	Pull up 10K ohm	TX_HALF_SWING	Controls the transmitter full/half swing mode. 0: The transmitter full swing is enabled. 1: The transmitter half swing is enabled.
GPIO 22	Pull low 10K ohm	BIOS_ROM_EN	Enable external BIOS ROM device. 0: Disable external BIOS ROM device. 1: Enable external BIOS ROM device.
GPIO 11	Pull up 10K ohm	ROM_CONFIG[2:0]	b) if BIOS_ROM_EN = 0, then ROM_CONFIG[2:0] defines the primary memory aperture size. GPIO_[13:12:11]=001=256MB
GPIO 12	Pull low 10K ohm		
GPIO 13	Pull low 10K ohm		
Hsync	NC	Reserve	Reserve
Vsync	NC		
DBGDATA2	Pull up 10K ohm	AUD_PORT_CONN [2:0]	Determine the maximum number of digital display audio endpoints 101: Two usable endpoints
DBGDATA1	Pull low 10K ohm		
DBGDATA0	Pull up 10K ohm		
GPIO 1	Pull up 10K ohm	SMBUS_ADDR	Provide a strap option to change the SMBUS slave address of the GPU. 0: 0x40 1: 0x41
GPIO 2	Pull up 10K ohm	BIF_GEN3_EN_A	PCIe Gen3 capability. 1: PCIe Gen3 is supported. 0: PCIe Gen3 is not supported.
GPIO 8	connect CLKREQ#_GPU and add pull up / down resistor	BIF_CLK_PM_EN (Reserve)	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0: The CLKREQB power management capability is disabled. 1: The CLKREQB power management capability is enabled.
WAKEB	Pull low 10K ohm	OBFF	0: Disable
SVI2_SVC	Pull up 1Kohm	Boot up voltage	SVC:SVD=[1:0]=0.90V
SVI2_SVD	Pull low 1K ohm		

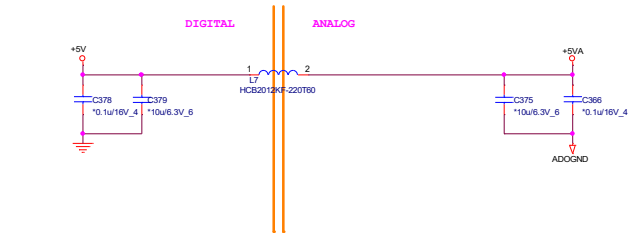




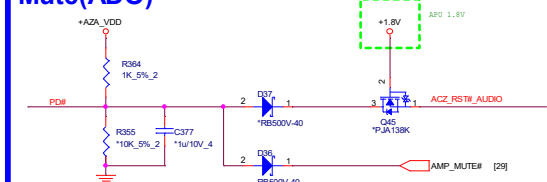
Codec PWR 1.5V(ADO)



Codec PWR 5V(ADO)



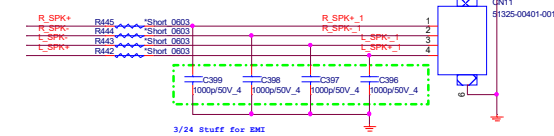
Mute(ADO)



Internal Speaker

4 ohm : 40mil for each signal

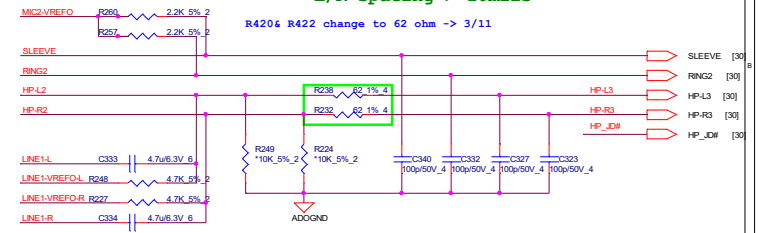
40mil for each signal

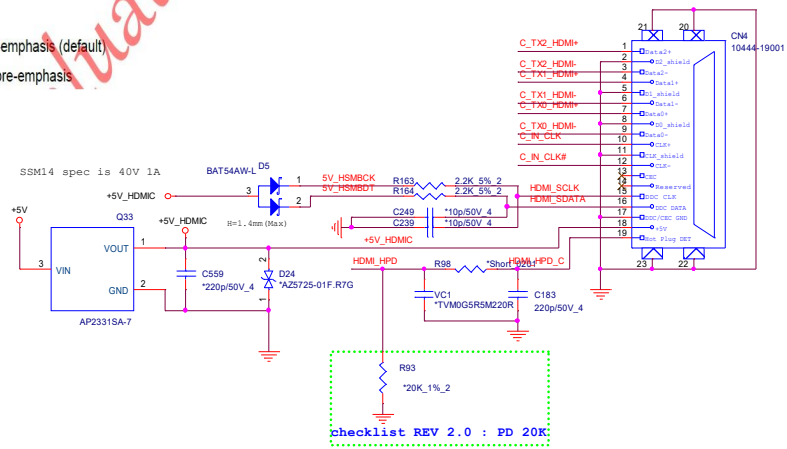


Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)

SLEEVE/RING2 trace > 40mils
HP/LINE trace > 10mils
L/R spacing > 10mils

R420& R422 change to 62 ohm -> 3/11





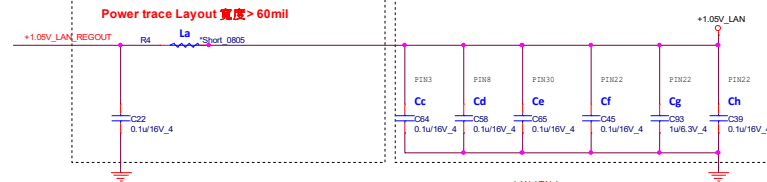
The schematic shows a +3V supply rail connected to a series of components. The components are connected in parallel to the rail and ground. The components are: C212, HDMI_R, C558, HDMI_R, C210, HDMI_R, C182, HDMI_R, C222, HDMI_R, C180, HDMI_R, and C181, HDMI_R. Each component is connected to ground.

ESD				
C_TX0_HDMI-	D32	2	1	*PESD5V0H1BSF
C_TX0_HDMI+	D31	2	1	*PESD5V0H1BSF
C_TX1_HDMI-	D30	2	1	*PESD5V0H1BSF
C_TX1_HDMI+	D29	2	1	*PESD5V0H1BSF
C_TX2_HDMI-	D28	2	1	*PESD5V0H1BSF
C_TX2_HDMI+	D27	2	1	*PESD5V0H1BSF
C_IN_CLKB	D26	2	1	*PESD5V0H1BSF
C_IN_CLK	D25	2	1	*PESD5V0H1BSF
HDMI_SCLK	D3	2	1	*PESD5V0H1BSF
HDMI_SDATA	D4	2	1	*PESD5V0H1BSF

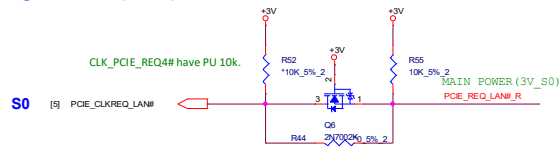
For LDO mode support
RTL8107ESH-CG/RTL8111HSH-CG
Stuff: La, Ca, Cb

* Place Cc,Cd,Ce,Cf for RTL8107ESH-CG/RTL8111HSH-CG
close to each VDD10 pin-- 3, 22, 8, 30

* Place Cg,Ch for RTL8107ESH-CG/RTL8111HSH-CG
close to each VDD10 pin-- 22(reserved)

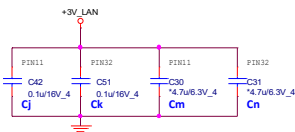


Leakage circuit (MPC)

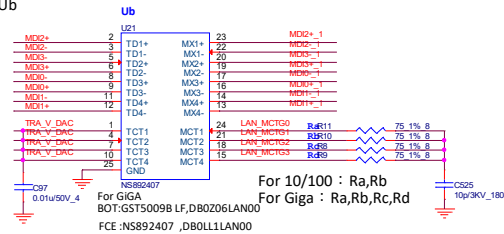


* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for
RTL8107ESH-CG/RTL8111HSH-CG

* For surge improvement, place Cm and Cn, close to each
VDD33 pin-- 11, 32(optional)

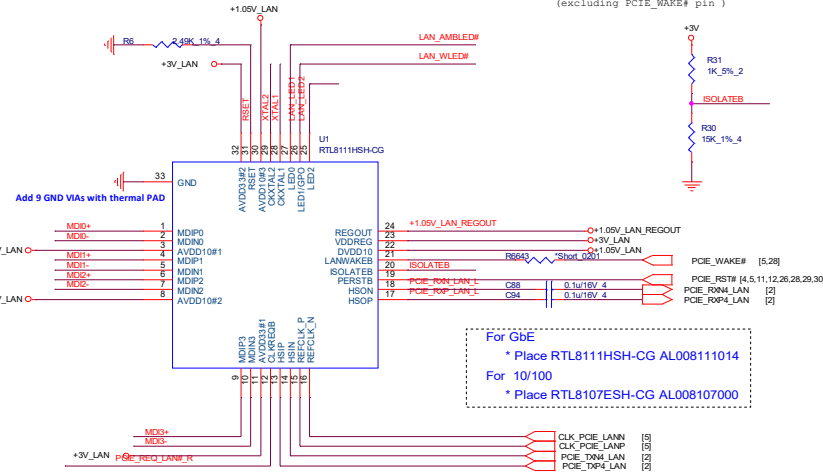


For Giga : Ub

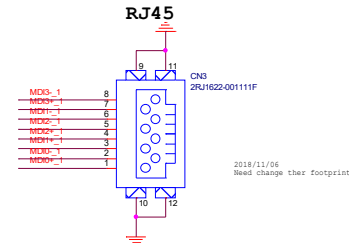


LAN_AMBLEDF# TP4
LAN_LED1 TP2
LAN_LED2 TP3

if ISOLATEB pin pull-low,
the LAN chip will not drive it's PCI-E outputs
(excluding PCIE_WAKE# pin)

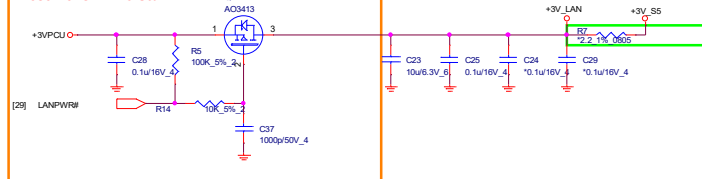


For GbE
* Place RTL8111HSH-CG AL008111014
For 10/100
* Place RTL8107ESH-CG AL008107000

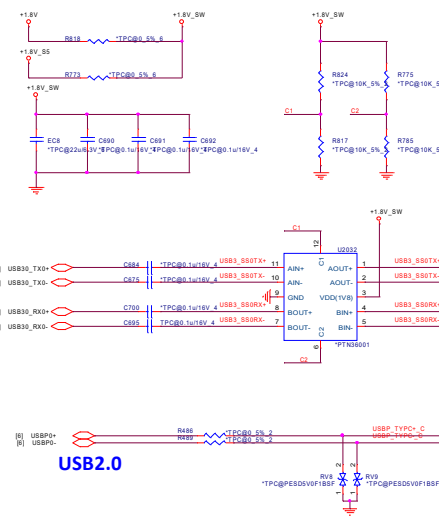


2018/11/06
Need change their footprint

Reserve IOAC No Stuff

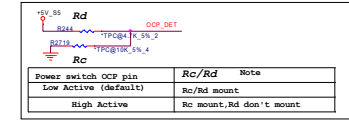
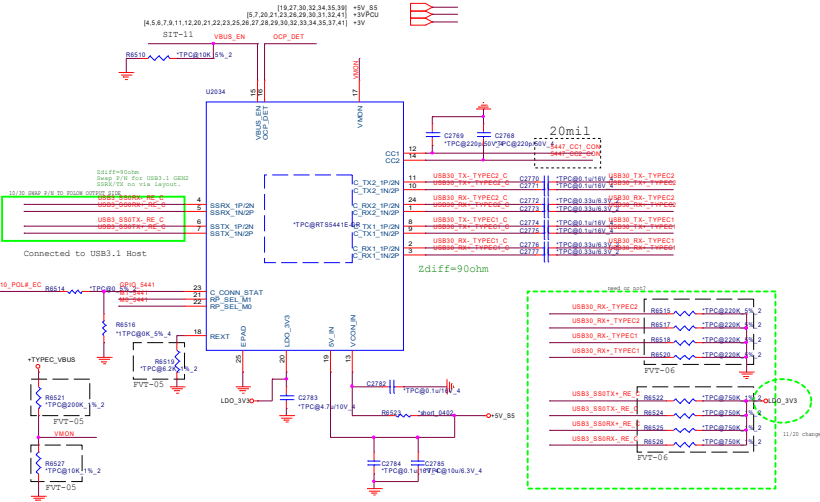


TYPE C and MUX PI2EQX632EXUBE



8.4 C1 and C2 overall control table

C1	C2	EQ		DE		OS		CEU
		Channel A	Channel B	Channel A	Channel B	Channel A	Channel B	
HIGH	HIGH	9 dB	9 dB	-5 dB	-5 dB	1.1 V	1.1 V	1
HIGH	OPEN	6 dB	9 dB	-5 dB	-3 dB	1.1 V	10 V	1
HIGH	LOW	3 dB	9 dB	-5 dB	-3 dB	1.1 V	0.9 V	1
OPEN	HIGH	9 dB	6 dB	-3 dB	-5 dB	10 V	1.1 V	1
OPEN	OPEN	6 dB	6 dB	-3 dB	-3 dB	10 V	10 V	1
OPEN	LOW	3 dB	6 dB	-3 dB	-5 dB	10 V	0.9 V	1
LOW	HIGH	9 dB	3 dB	0 dB	-5 dB	0.9 V	1.1 V	1
LOW	OPEN	6 dB	3 dB	0 dB	-5 dB	0.9 V	10 V	1
LOW	LOW			Deep power-saving mode				0



For C_VBSS power switch OCP pin

Re

RS12 170K Ohm RS13 10K Ohm RS14 10K Ohm RS15 10K Ohm

M0_5441

Re configuration

	M0_5441	M0_5441	Note
Rp: 90 Ohm	0	1	Re/Rg mount, Re/Rh don't mount
Rp: 1.5 A	1	0	Re/Rh mount, RE/Rh don't mount
Rp: 3.0 A	1	1	Re/Rg mount, RE/Rh don't mount

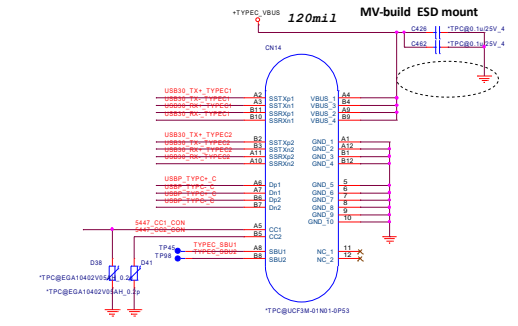
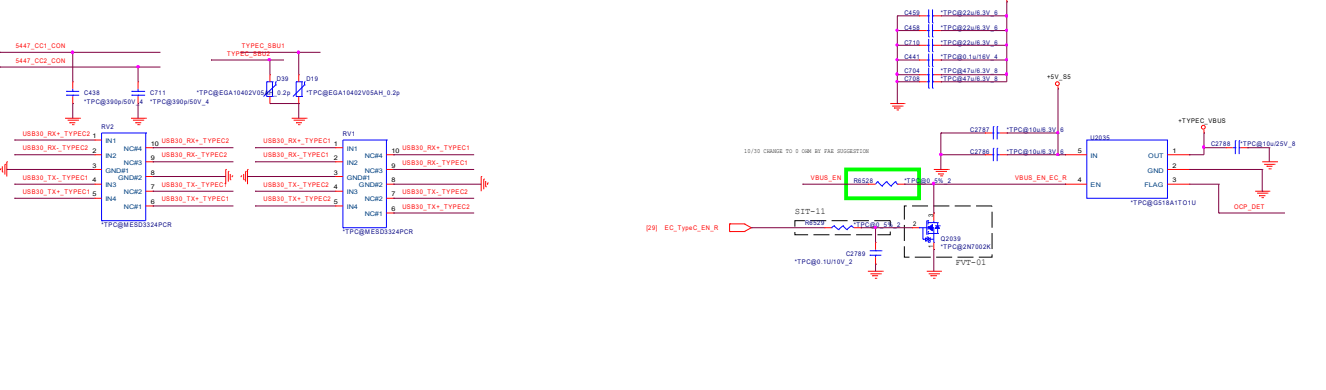
If can identify port1 or 2

```
25810 pol# EC
      (to EC invert)
L: Port1
H: Port2
```

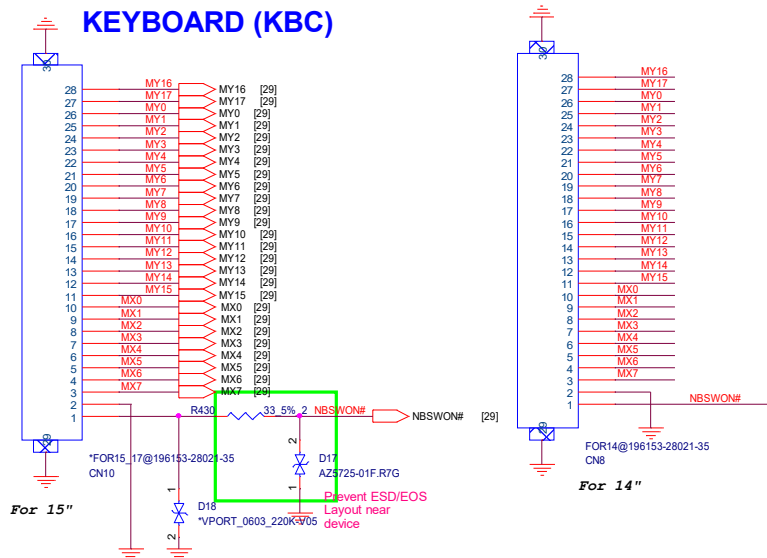
3V
50
R284
1k
FVT-05
25810_POL#_EC

to indicate attached state
1: Type-C is connected and under Attached.SRC state
0: Type-C is not connected and under Unattached.SRC state

TYPE C USB3.0 ESD

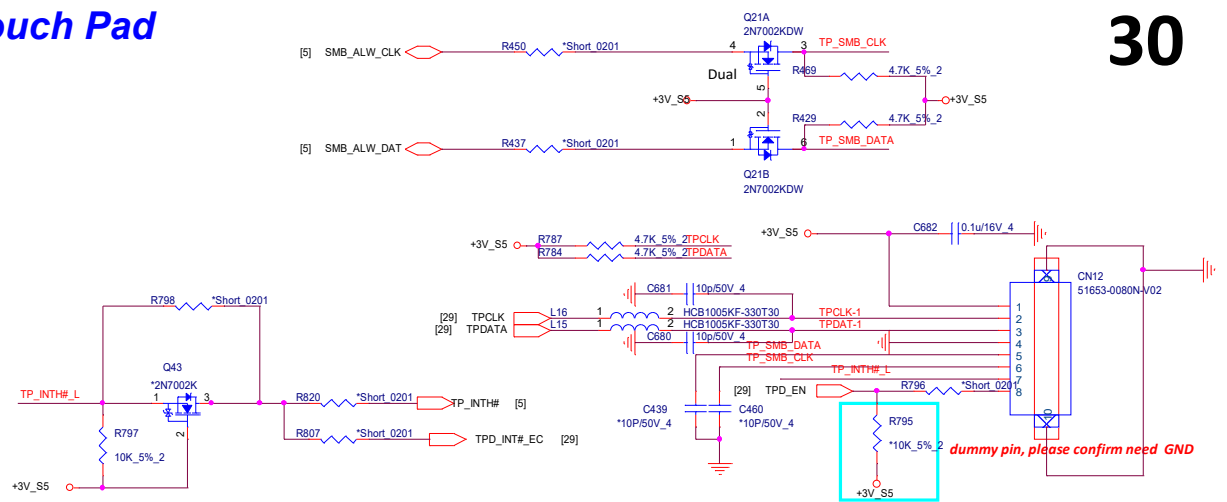


KEYBOARD (KBC)

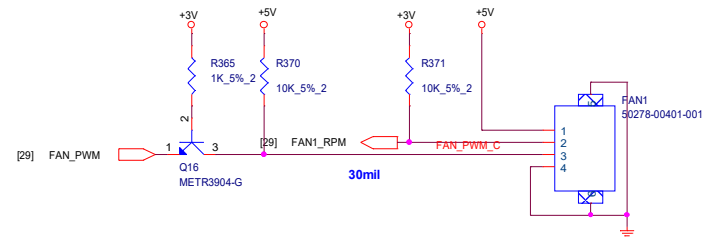


MY5	C414	220p/25V_2
MY6	C415	220p/25V_2
MY3	C410	220p/25V_2
MY7	C416	220p/25V_2
MY8	C417	220p/25V_2
MY9	C419	220p/25V_2
MY10	C418	220p/25V_2
MY11	C420	220p/25V_2
MY1	C408	220p/25V_2
MY2	C409	220p/25V_2
MY4	C411	220p/25V_2
MY0	C407	220p/25V_2
MX4	C405	220p/25V_2
MX6	C402	220p/25V_2
MX3	C404	220p/25V_2
MX2	C406	220p/25V_2
MX7	C403	220p/25V_2
MX0	C412	220p/25V_2
MX5	C401	220p/25V_2
MX1	C424	220p/25V_2
MY12	C421	220p/25V_2
MY13	C422	220p/25V_2
MY14	C423	220p/25V_2
MY15	C427	220p/25V_2
MY16	C400	220p/25V_2
MY17	C394	220p/25V_2

Touch Pad

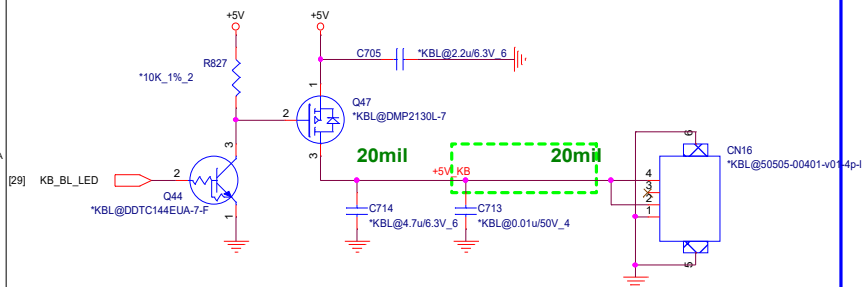


FAN check pin define

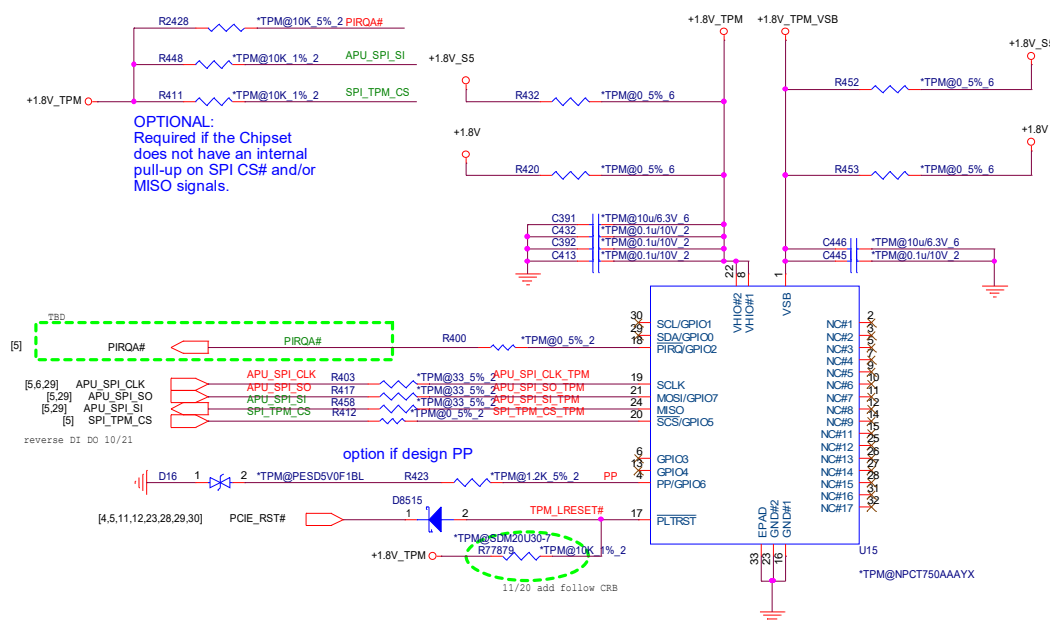


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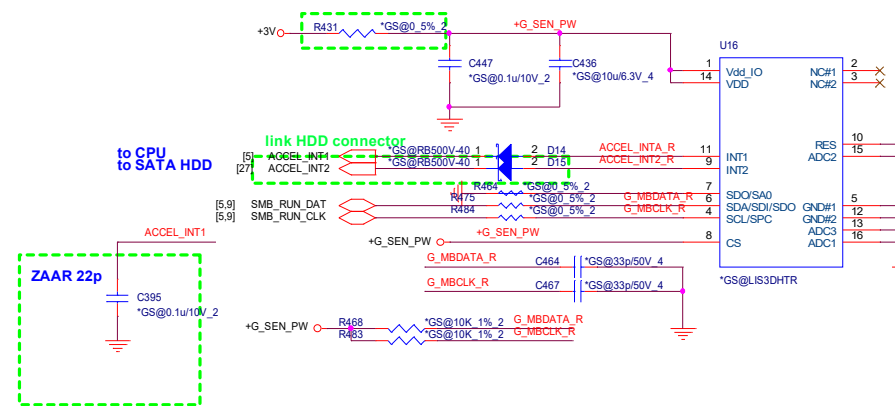
KB_BL LED (KBL@)



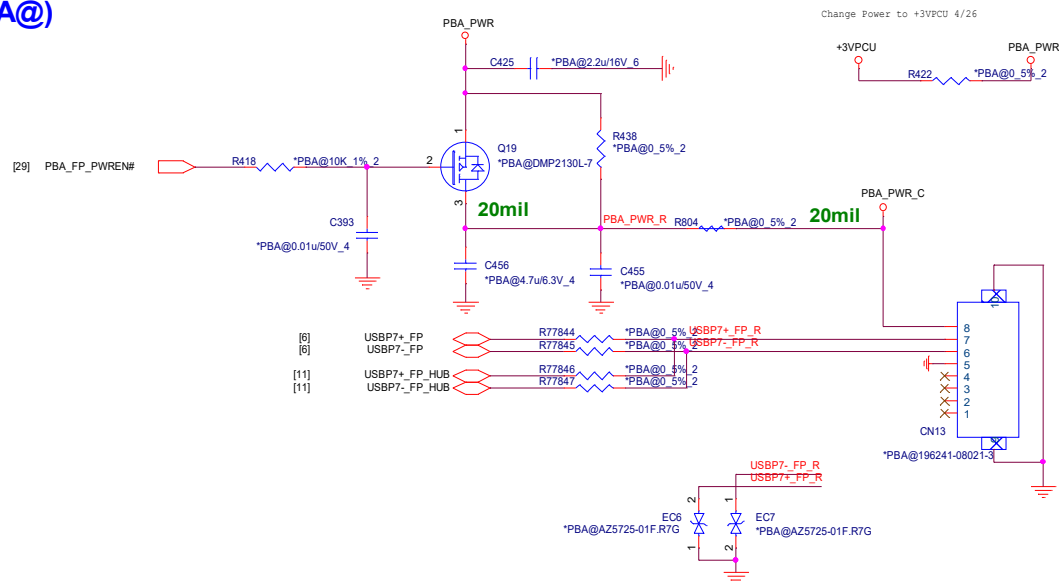
TPM NPCT750



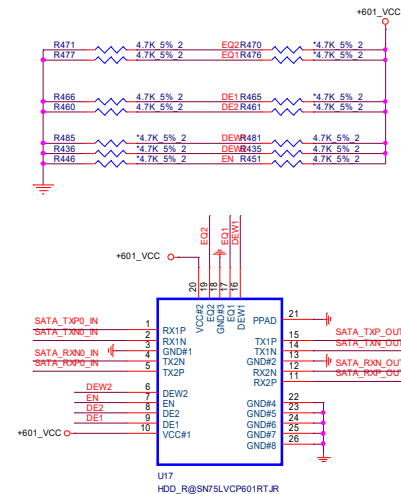
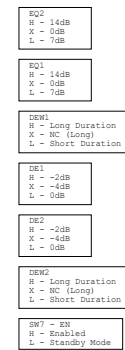
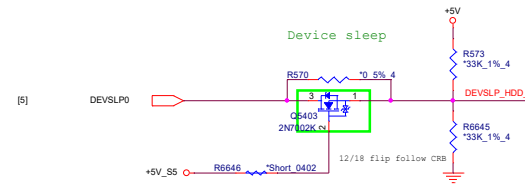
G-sensor (GS@)



PBA (PBA@)



	[19,24,30,32,34,35,39]	+5V_SS
	[20,21,22,25,30,32,37]	+5V
[4,5,6,7,9,11,12,20,21,22,23,24,25,26,28,29,30,32,33,34,35,37,41]		+3V
	[4,5,6,7,11,23,25,28,29,32,37,38]	+3V_SS



[illegible]

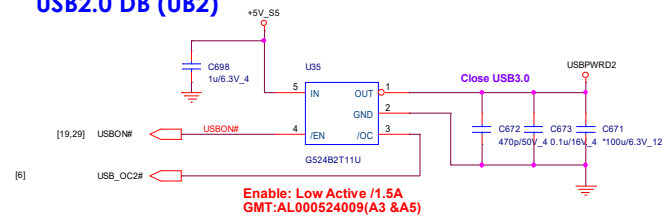
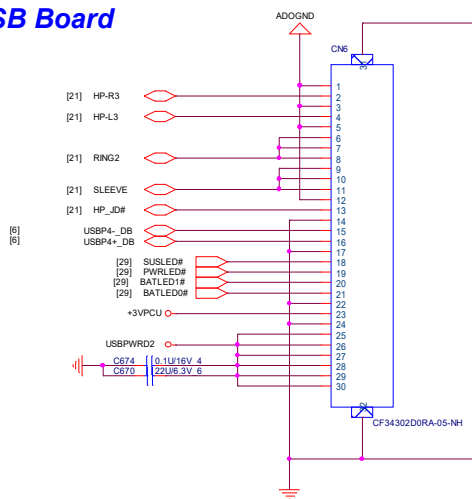
Figure 10 shows a timing diagram for a 100% duty cycle. The signal is high for the entire duration of the clock cycle. The signal is labeled "100% DUTY CYCLE" and "100% DUTY CYCLE".

[illegible]

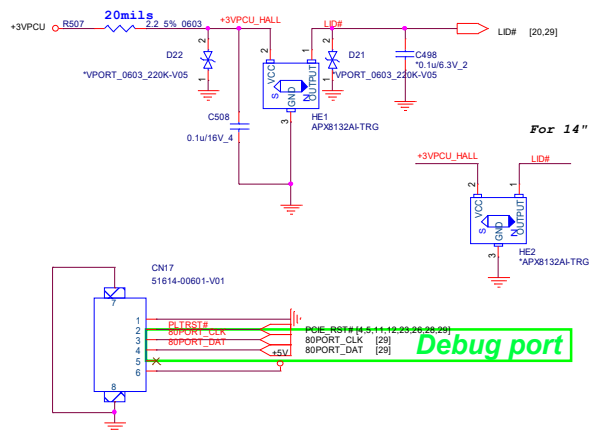
The schematic shows the APU SPI interface circuit. It includes two pull-up resistors (R6844 and R6843) connected to +1.8V_SS. The APU_SPI_HOLDIN pin is connected to the HOLDIN pin of the U2033B chip via a 10k resistor (R6832). The APU_SPI_CLK pin is connected to the CLK pin of the U2033B chip via a 22 ohm resistor (R6833). The APU_SPI_CS pin is connected to the CS pin of the U2033B chip via a 22 ohm resistor (R6830). The APU_SPI_MISO pin is connected to the MISO pin of the U2033B chip via a 22 ohm resistor (R6831). The APU_SPI_MOSI pin is connected to the MOSI pin of the U2033B chip via a 22 ohm resistor (R6834). The APU_SPI_SDO pin is connected to the SDO pin of the U2033B chip via a 22 ohm resistor (R6835). The APU_SPI_SDI pin is connected to the SDI pin of the U2033B chip via a 22 ohm resistor (R6836). The APU_SPI_SCK pin is connected to the SCK pin of the U2033B chip via a 22 ohm resistor (R6837). The APU_SPI_SCS pin is connected to the SCS pin of the U2033B chip via a 22 ohm resistor (R6838). The APU_SPI_SCS pin is also connected to the SCS pin of the U2033B chip via a 22 ohm resistor (R6839).



35



For 15"



DMIC

DMIC_CLK_2

DMIC_DAT_2_R

R77874

R77875

*Short_0201

*Short_0201

+3V_DMIC

DMIC_CLK_Z_R

DMIC_DAT_Z_R

CN1

*50208-00401-V02

4

3

2

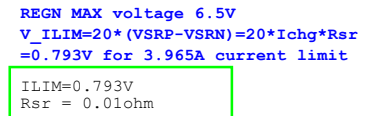
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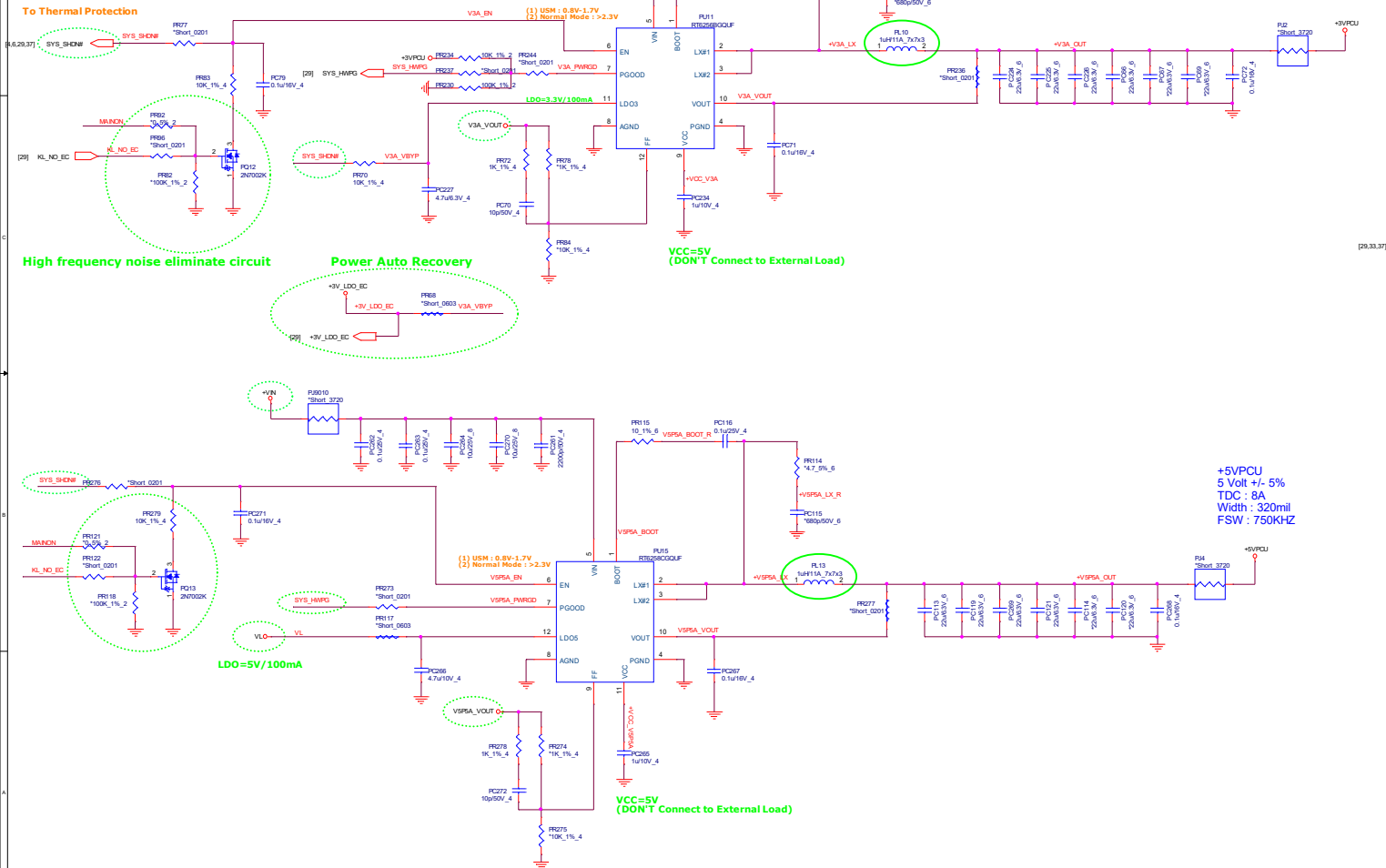
+3V

R514

*Short_0201

+3V_DMIC



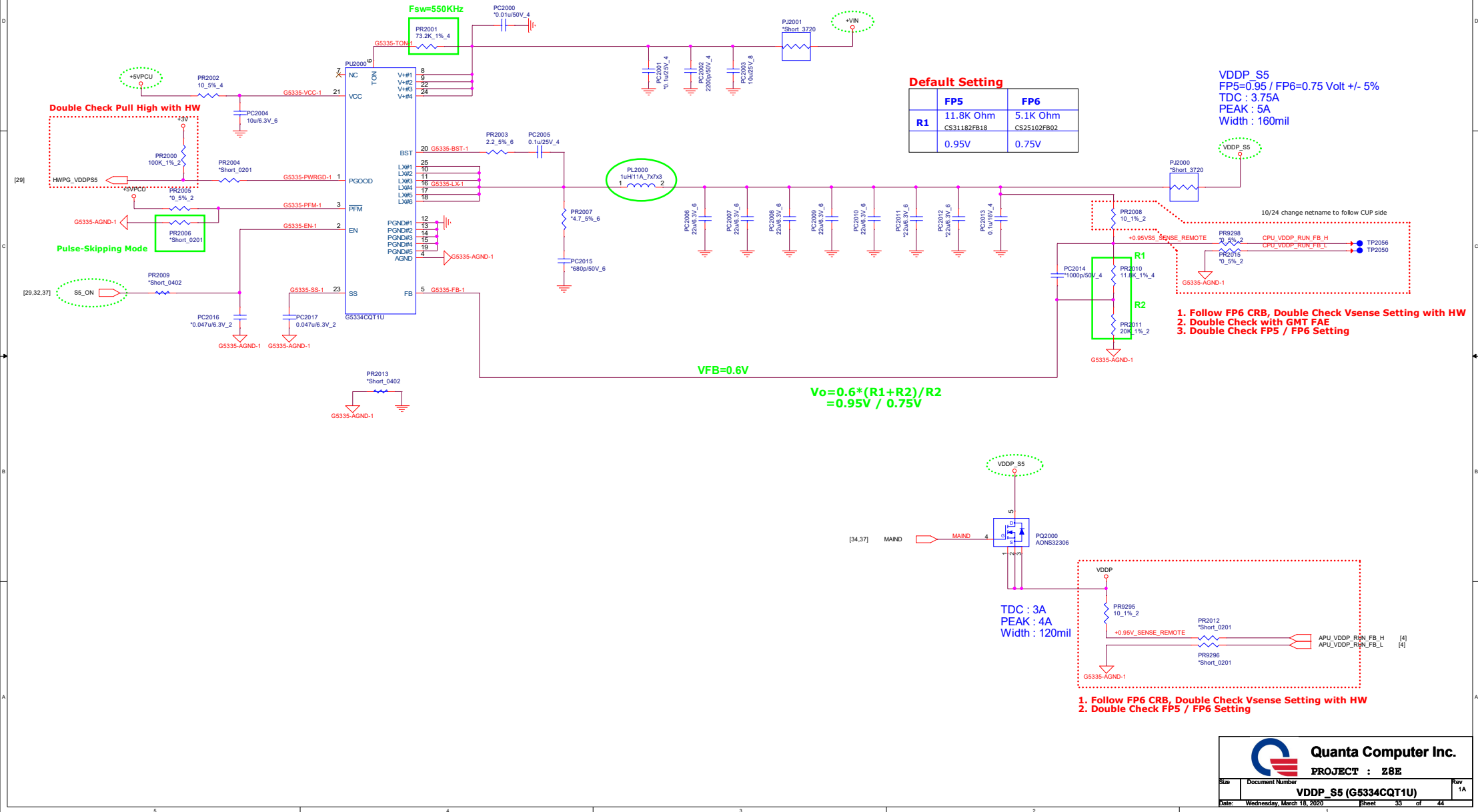


TDC : 4.58A
PEAK : 6.1A
Width : 200mil


TDC : 3.43A
PEAK : 4.6A
Width : 160mil

TDC : 4.54A
PEAK : 6A
Width : 200mil

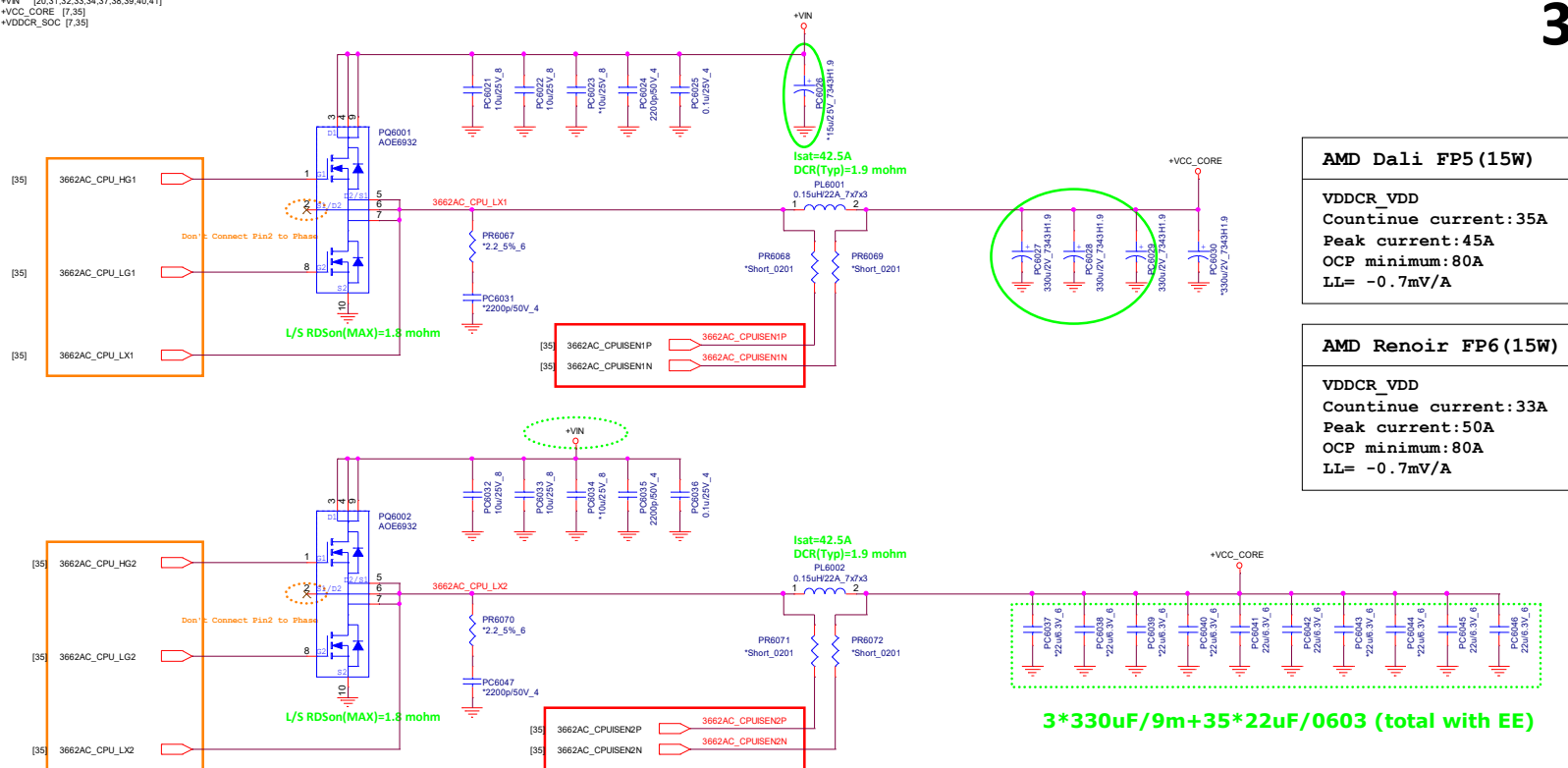
TDC : 3.53A
PEAK : 4.7A
Width : 160mil







+VIN [20,31,32,33,34,37,38,39,40,41]
+VCC_CORE [7,35]
+VDDCR_SOC [7,35]

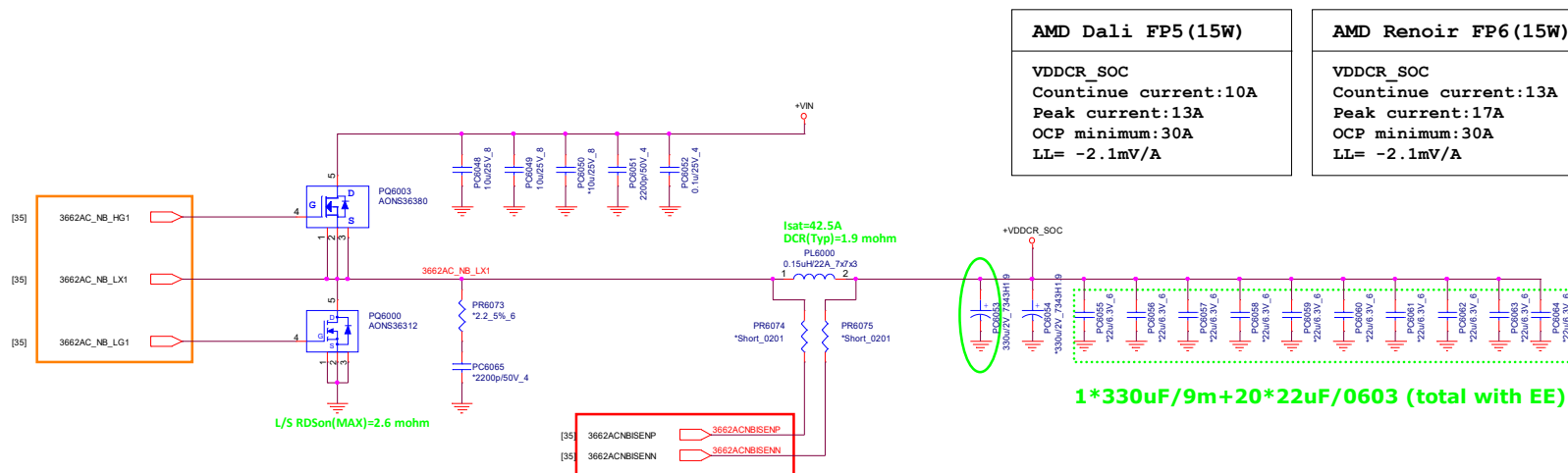


AMD Dali FP5 (15W)

```
VDDCR_VDD
Continue current:35A
Peak current:45A
OCP minimum:80A
LL= -0.7mV/A
```

AMD Renoir FP6 (15W)

```
VDDCR_VDD
Continue current:33A
Peak current:50A
OCP minimum:80A
LL= -0.7mV/A
```

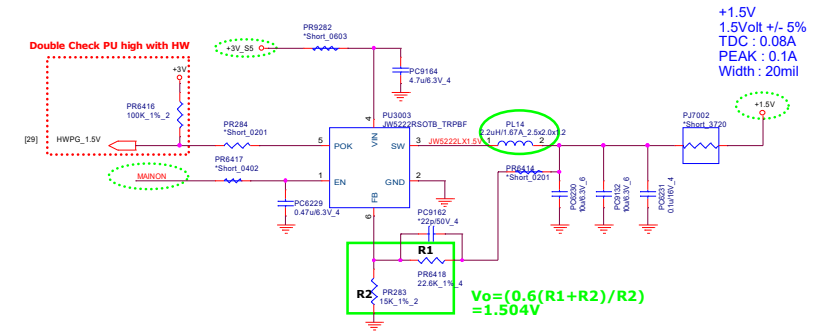
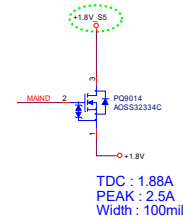


AMD Dali FP5 (15W)

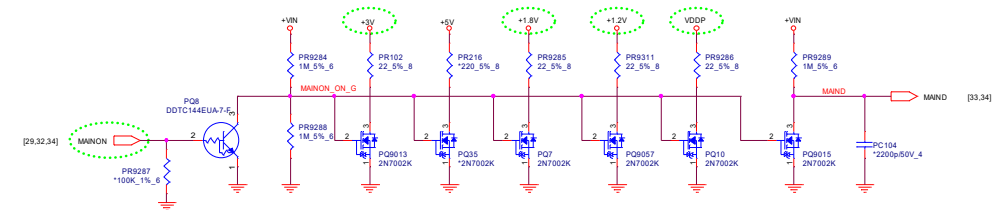
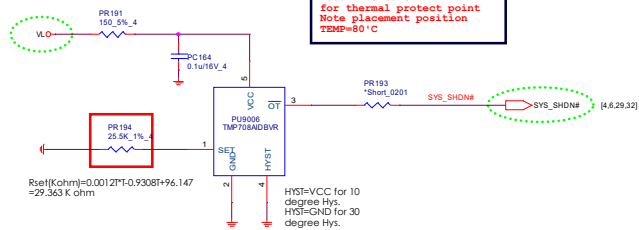
```
VDDCR_SOC
Countinue current:10A
Peak current:13A
OCP minimum:30A
LL= -2.1mV/A
```

AMD Renoir FP6 (15W)

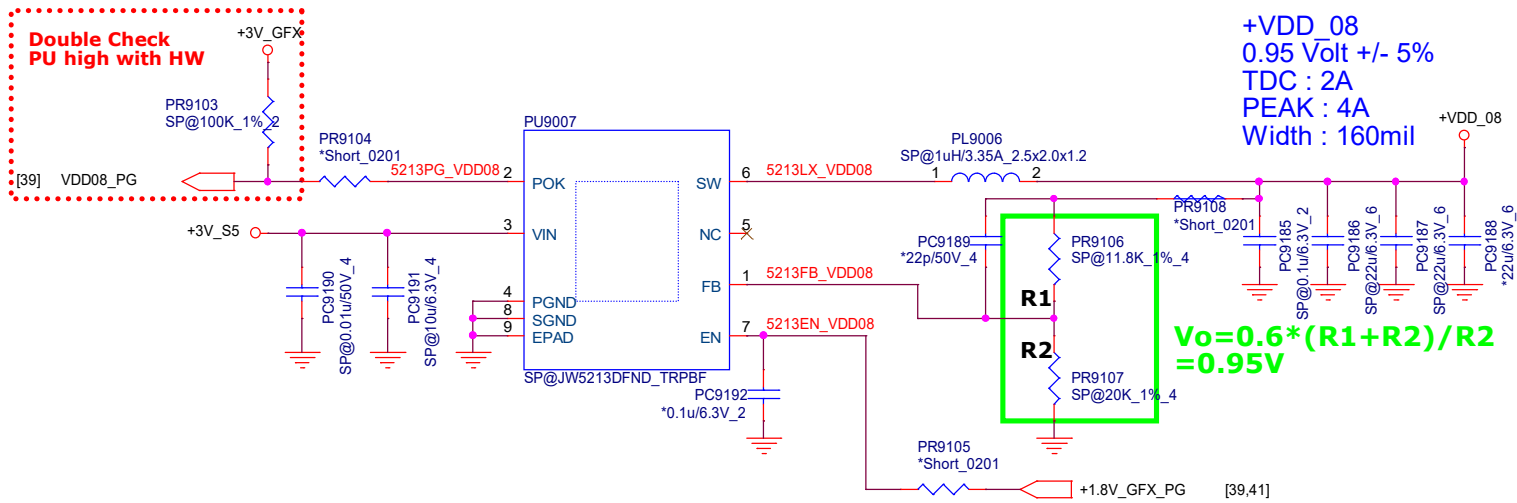
```
VDDCR_SOC
Continue current:13A
Peak current:17A
OCP minimum:30A
LL= -2.1mV/A
```



Need fine tune
for thermal protect point
Note placement position
TEMP=80'C



Design Reserved



R19M-P18-50 no stuff:
PR9103, PR9104, PC9190, PC9191, PU9007, PL9006, PR9106, PR9107, PR9105, PC9185, PC9186, PC9187

R19M-P18-50 stuff:
PJ9000, PC9046, PC9045, PC9043, PC9042, PQ9002, PL9002, PR9072, PR9073, PC9047, PC9049

+VDDCI (R19M-M18-50)_18W

VDD_08

Vo = 0.95V (Fix)

TDC : 2A

EDC : 3A

OCP : 16A

+VDDCI (R19M-P18-50)_18W

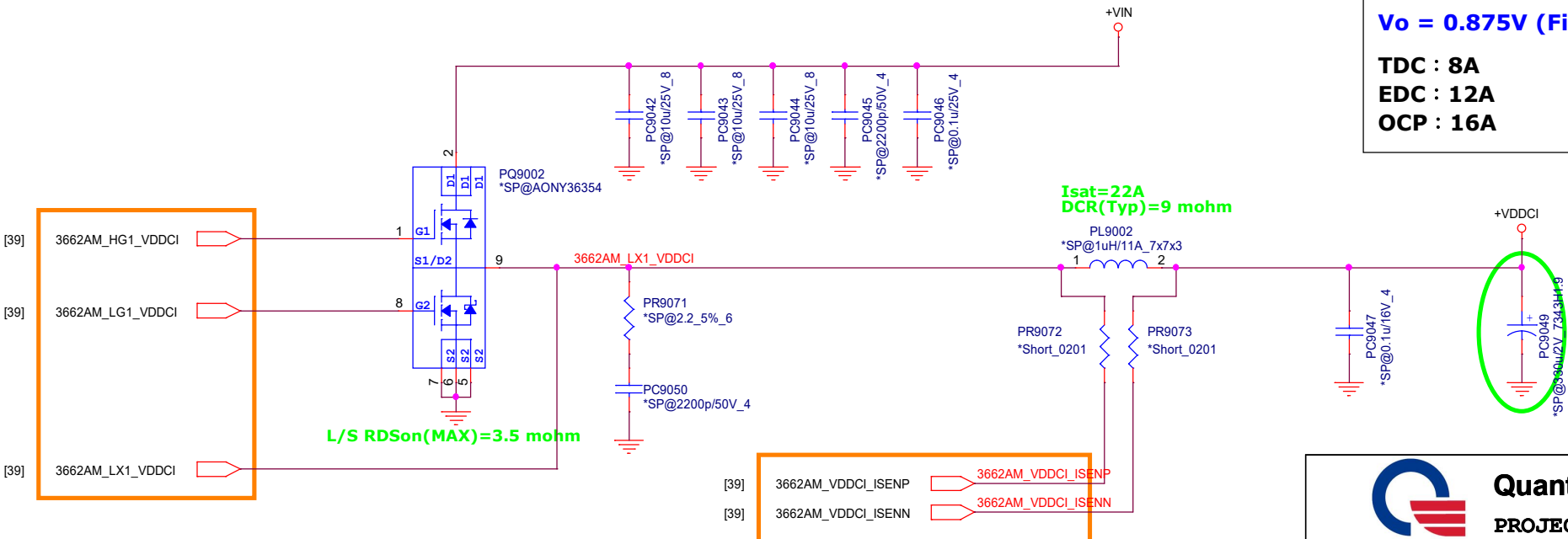
VDDCI + VDD_08 (merged)

Vo = 0.875V (Fix)

TDC : 8A

EDC : 12A

OCP : 16A



Quanta Computer Inc.

PROJECT :

LED Panel (TPS61087)

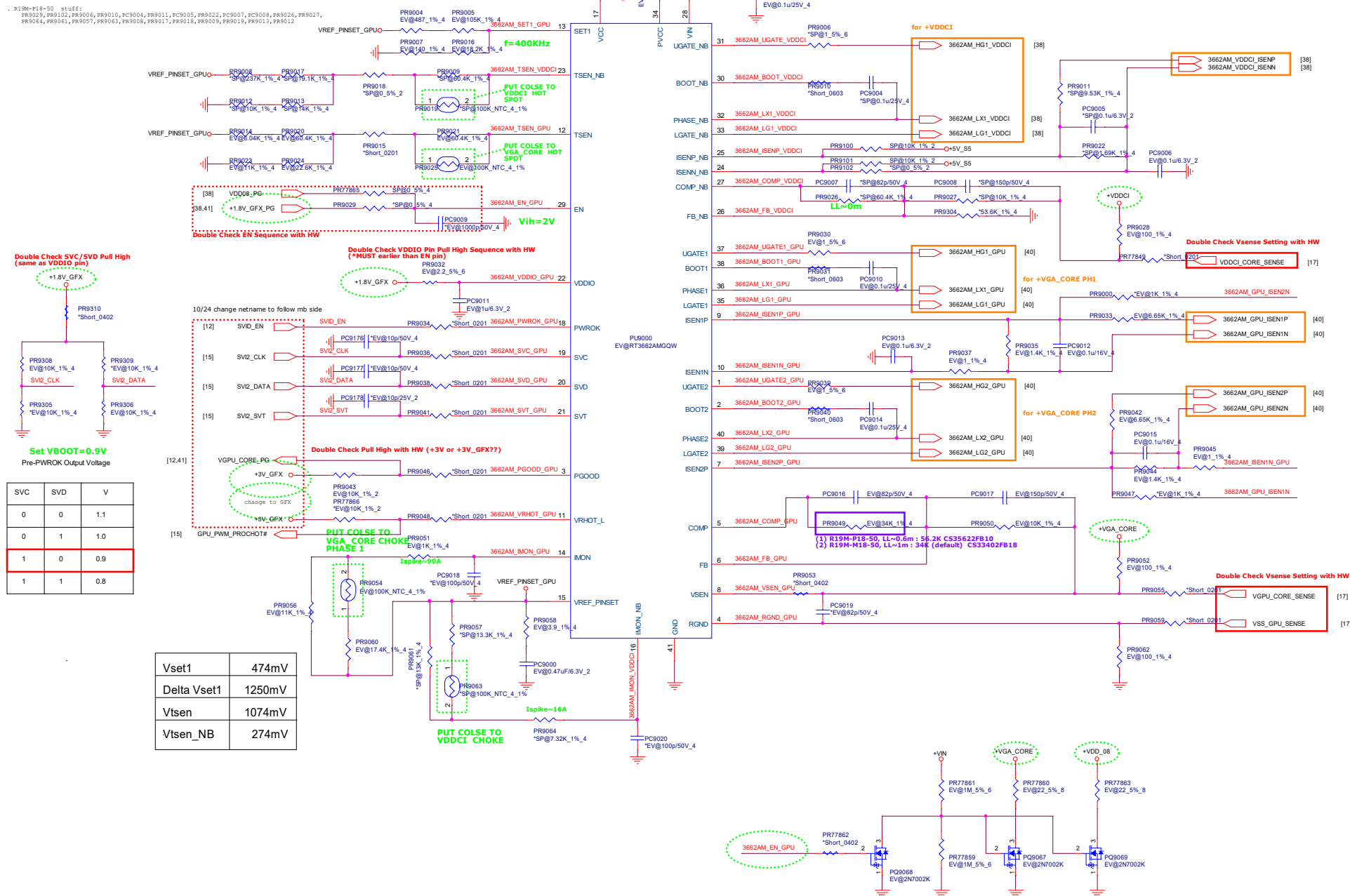
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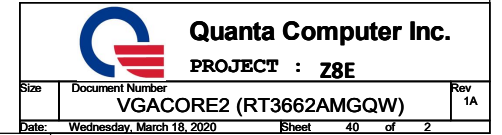
Date: Wednesday, March 18, 2020 Sheet 38 of 44

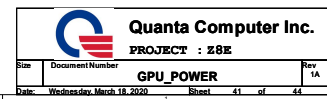
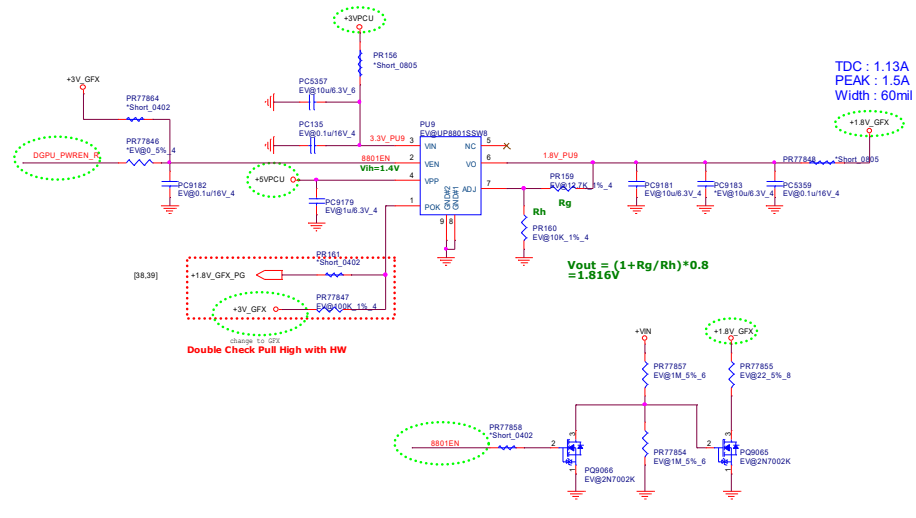
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FR9100,FR9101,FR77865

FR9100,FR9101,FR77865

R19M-F18-50 stuff:
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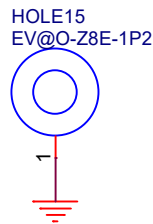
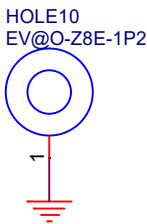
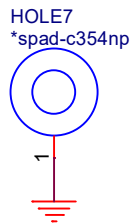
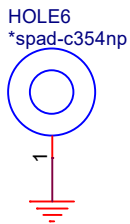
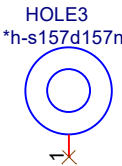
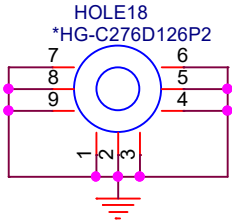
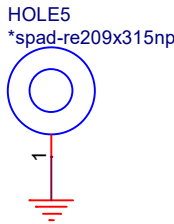
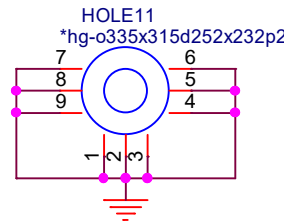
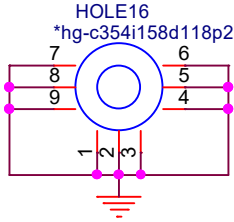
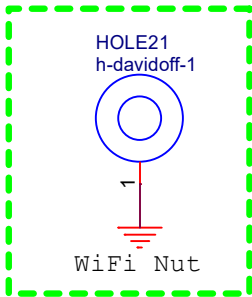
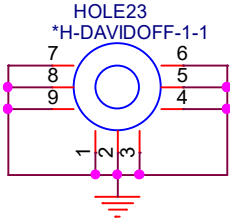
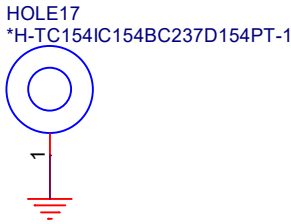
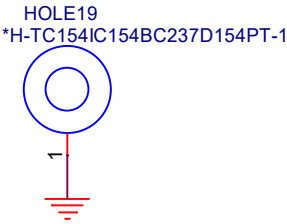
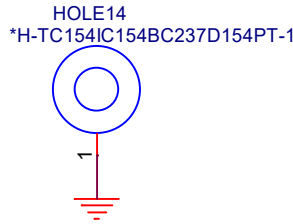
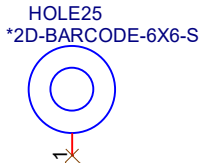
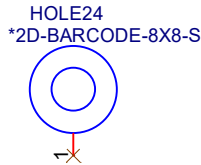
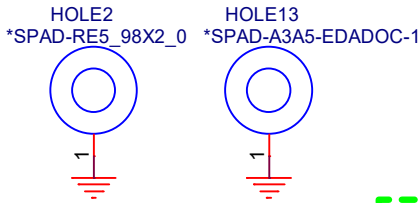
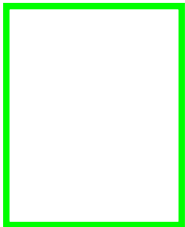
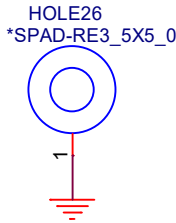
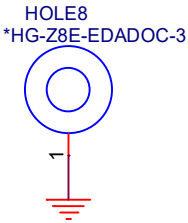
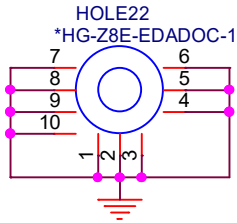




Hole

45

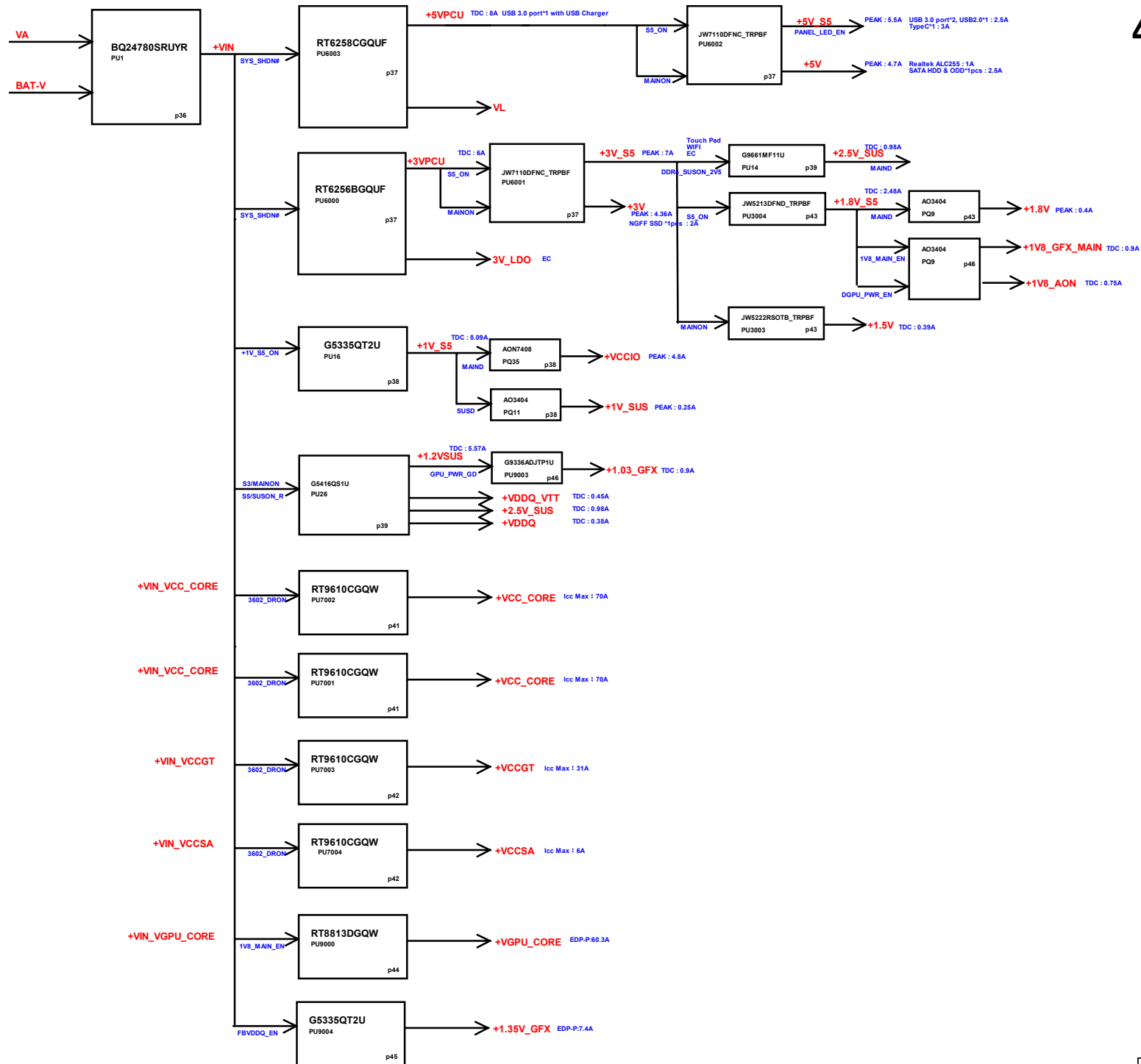
remove HOLE12 as Z8E



Quanta Computer Inc.

PROJECT : Z8E

Size	Document Number	Rev
	Hole	1A
Date:	Wednesday, March 18, 2020	Sheet 42 of 44



Stage	Date	CHANGE LIST
A	20191005	1.first released
C		
MP		